AGILE: Lightweight and Efficient Asynchronous GPU-SSD Integration

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AGILE is open source!

https://peipeizhou-eecs.github.io/

https://github.com/arc-research-lab/AGILE

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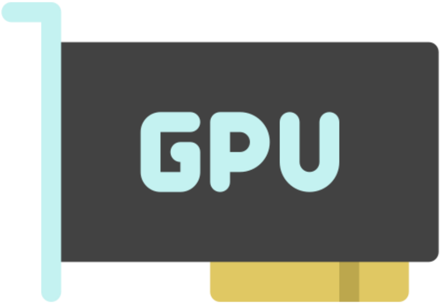
Syracuse University



GPGPU: The engine behind modern applications.

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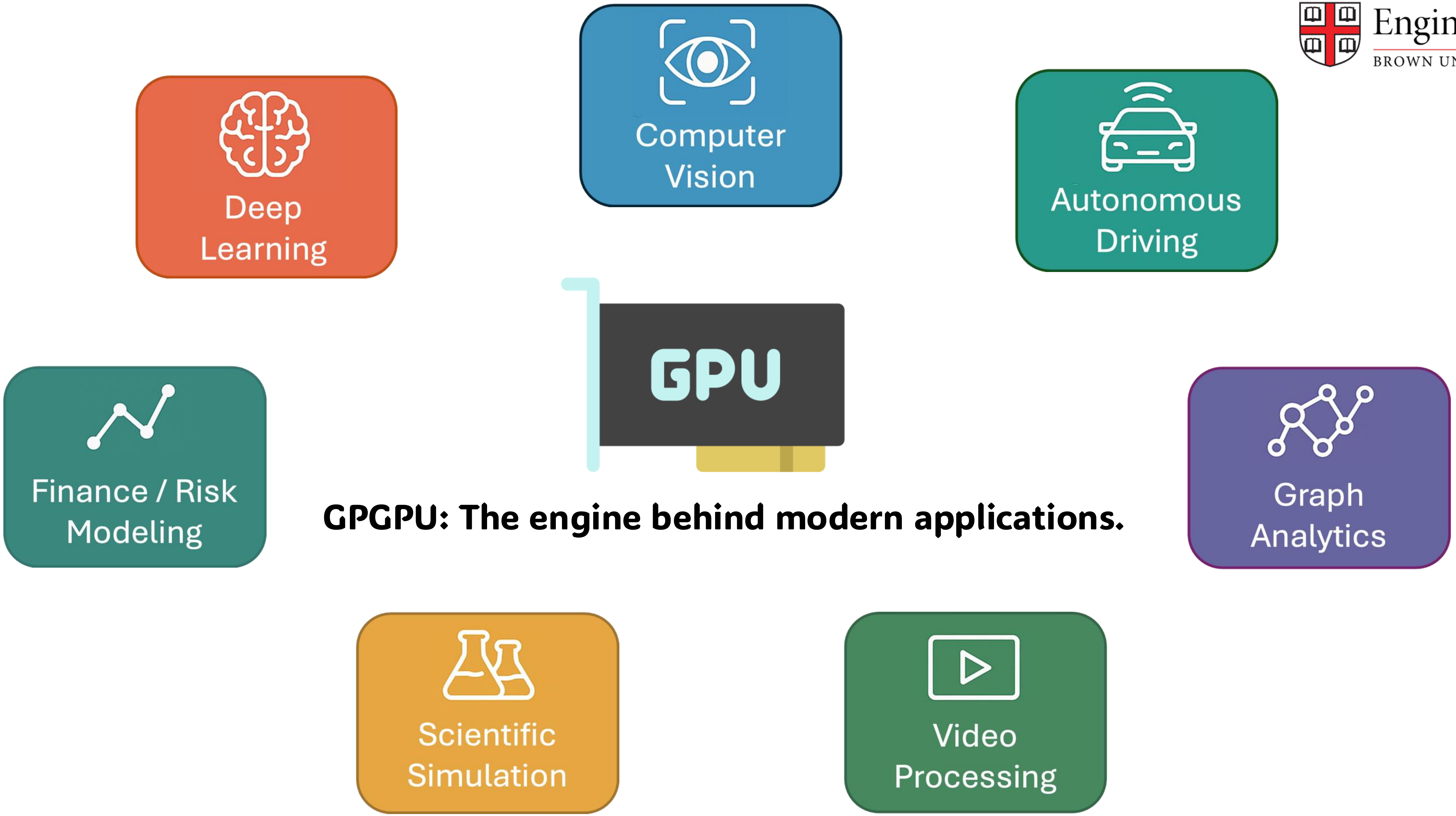

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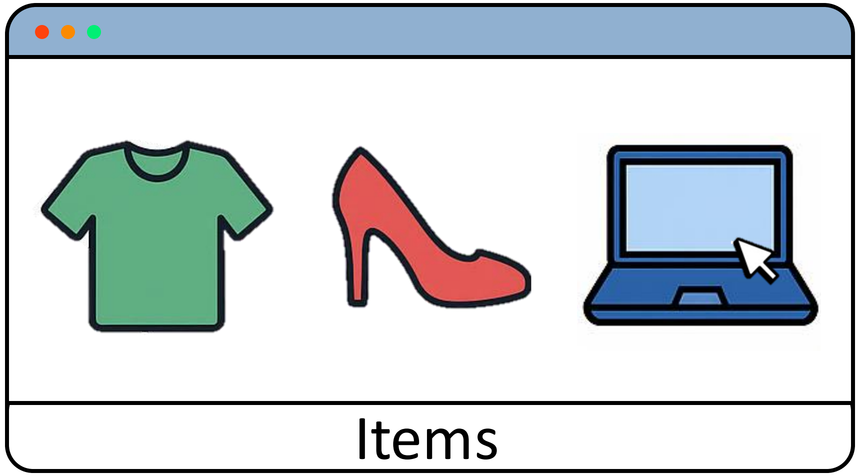
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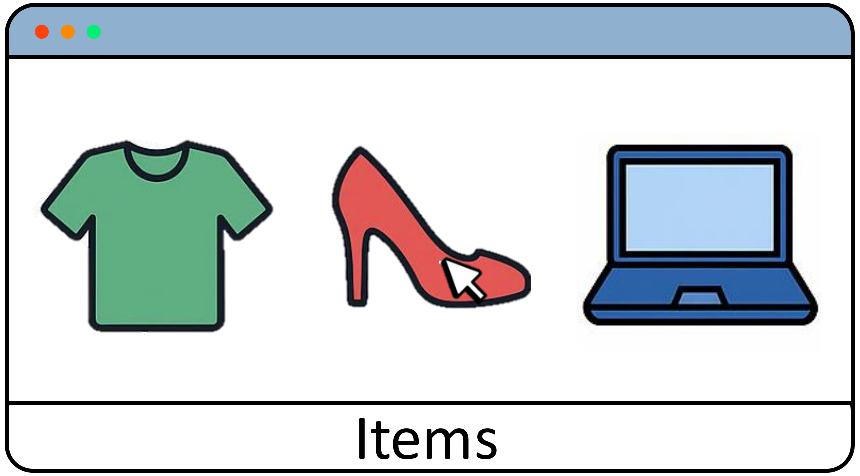
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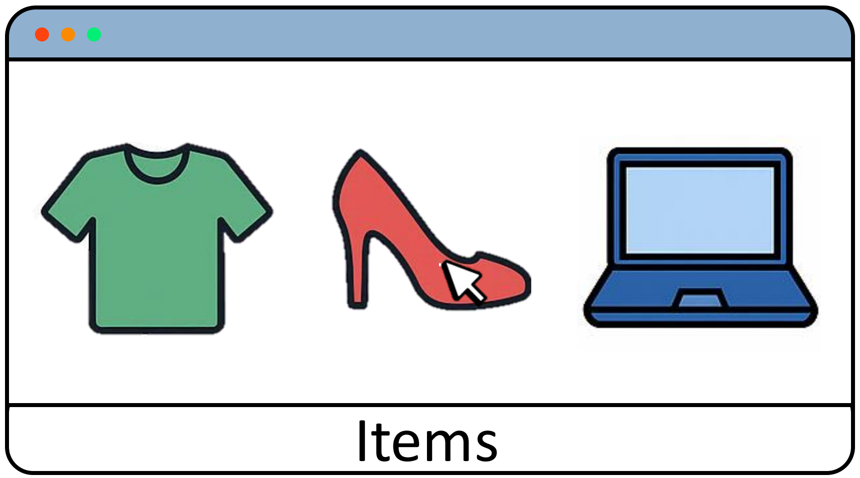
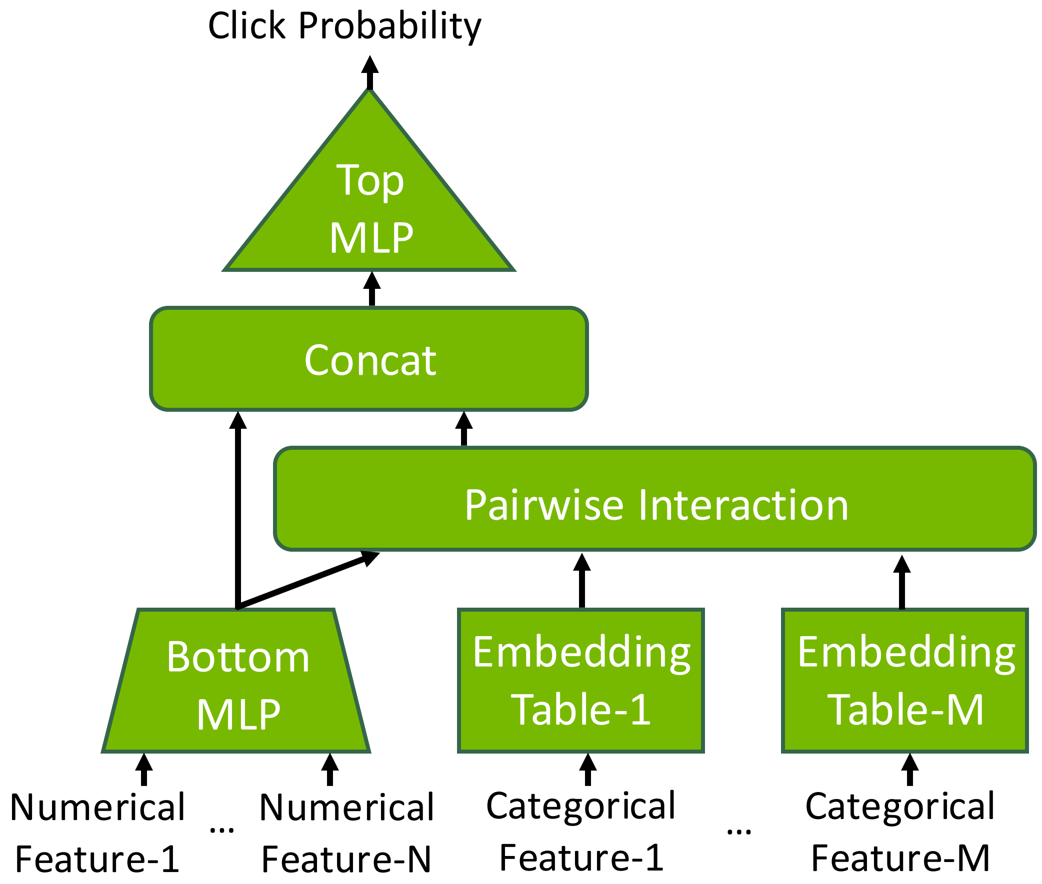
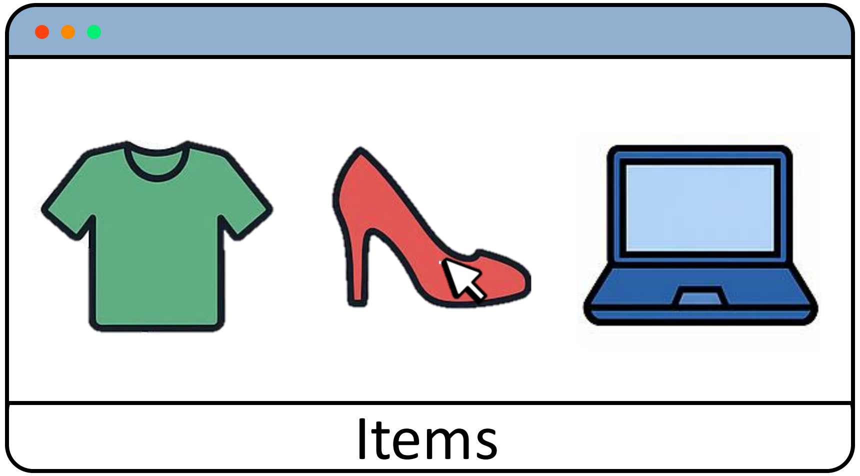
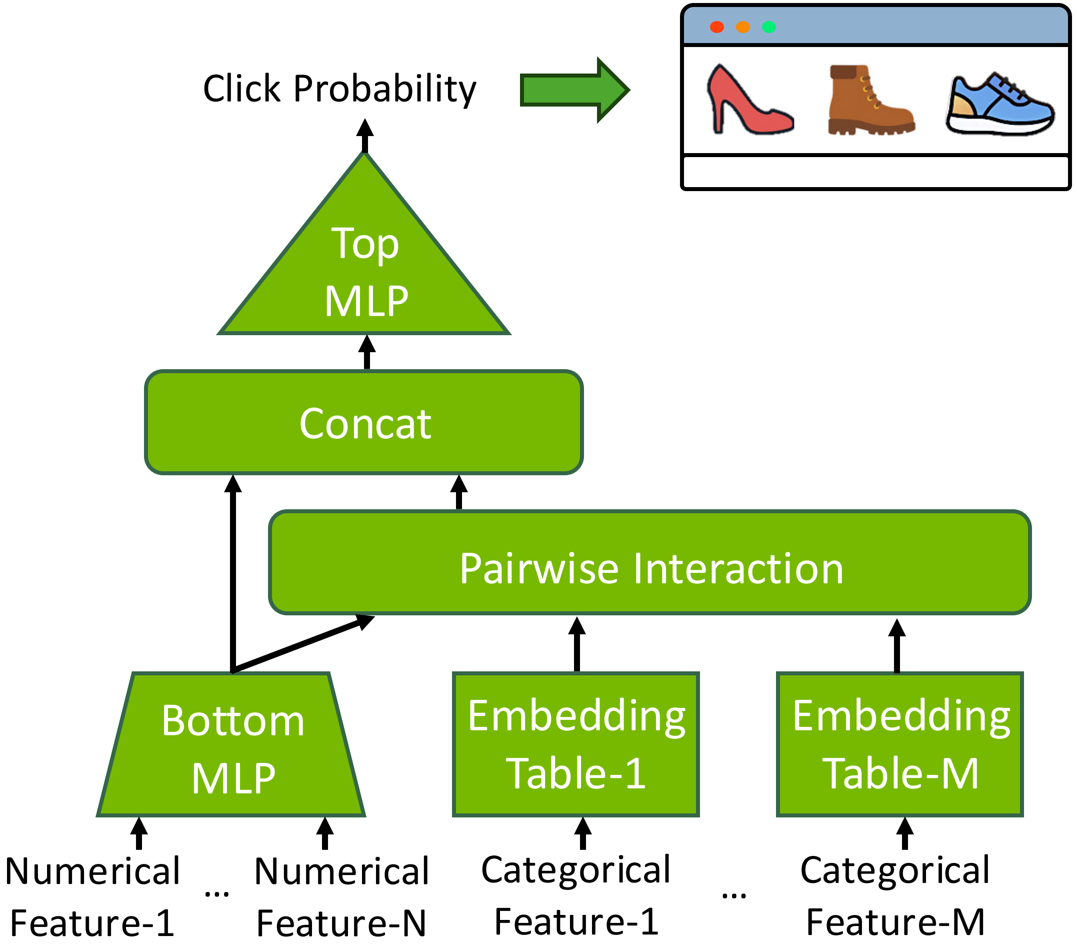




Recommendation System





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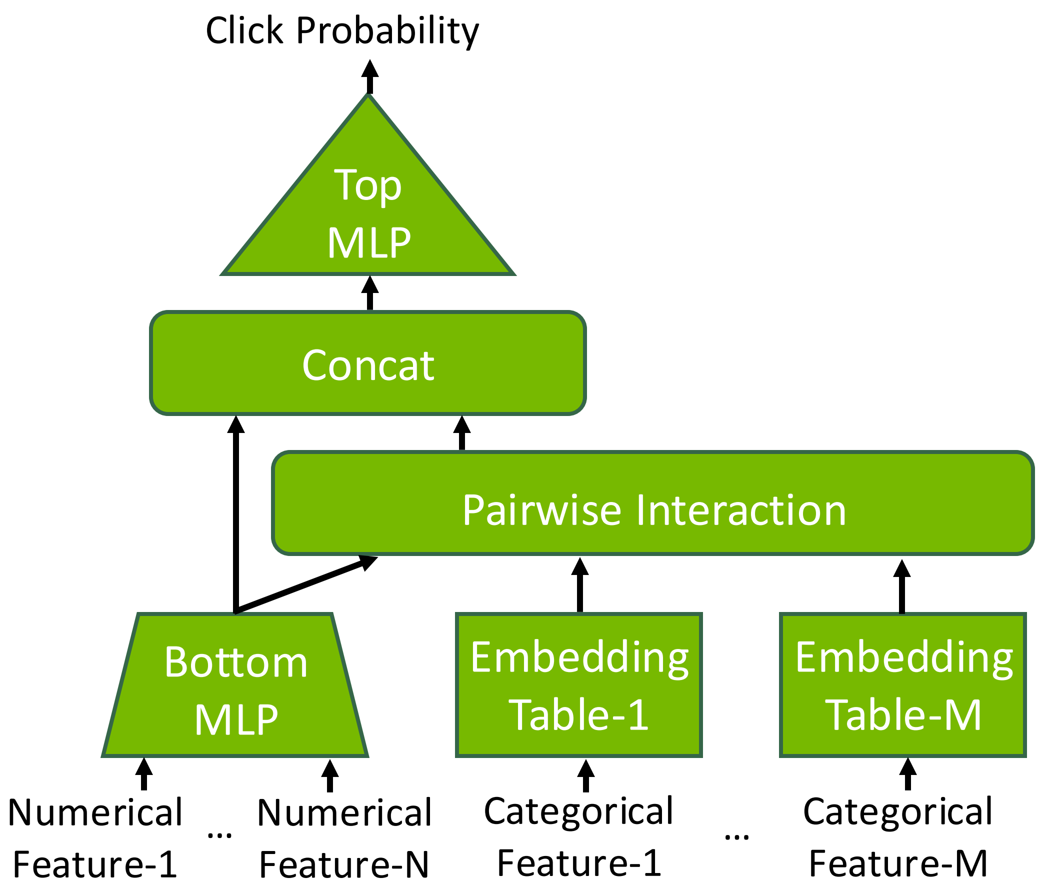

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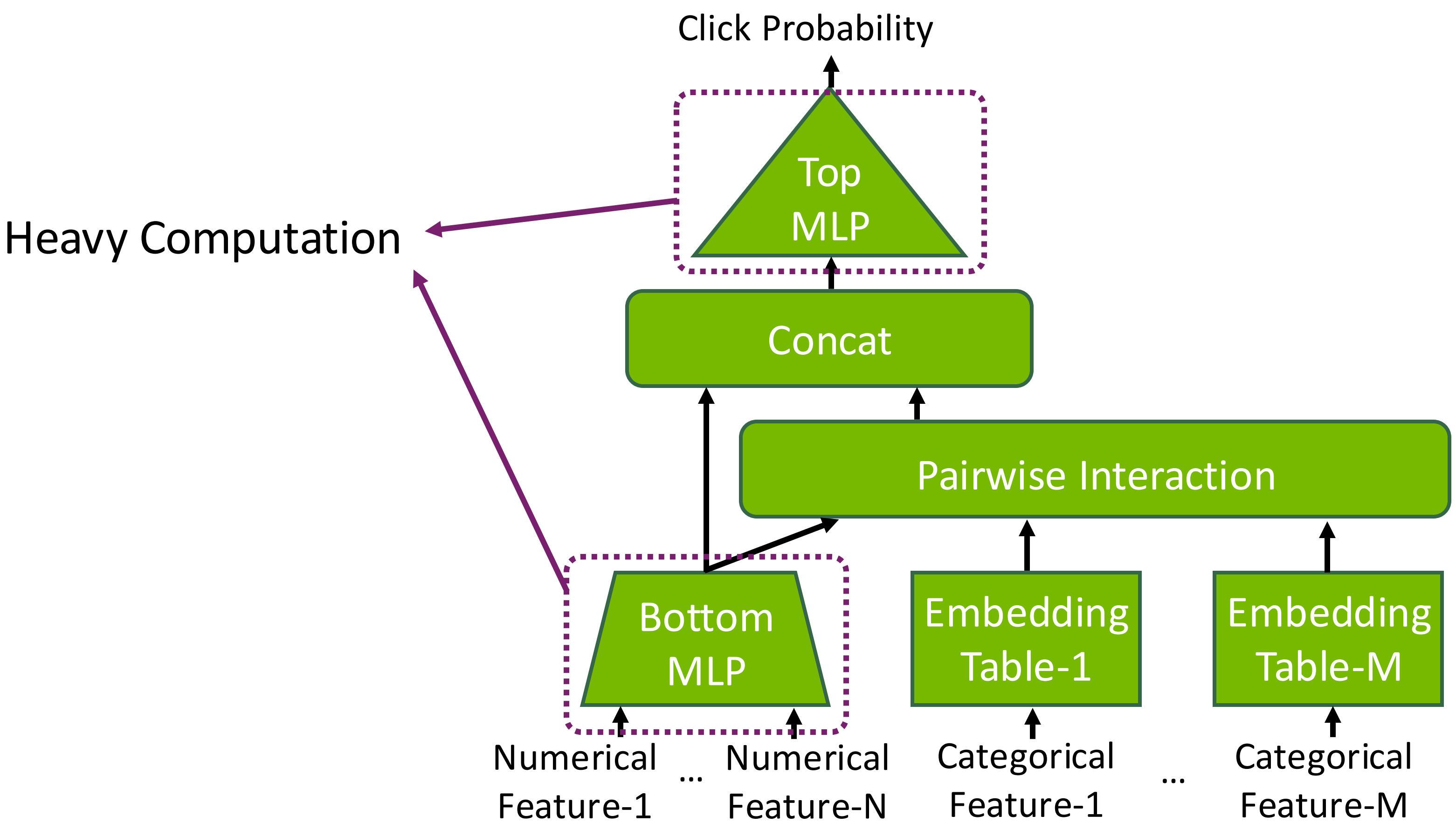

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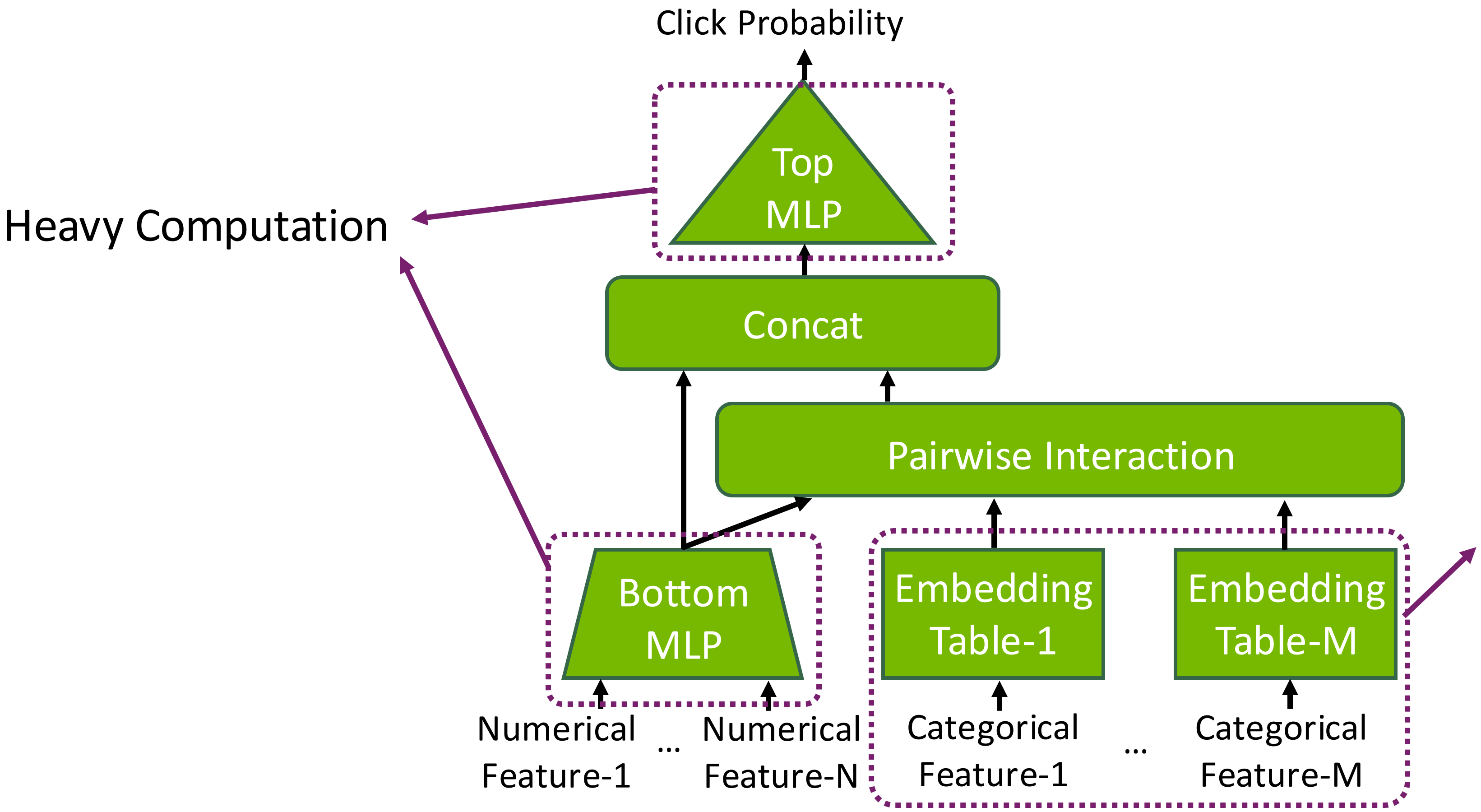
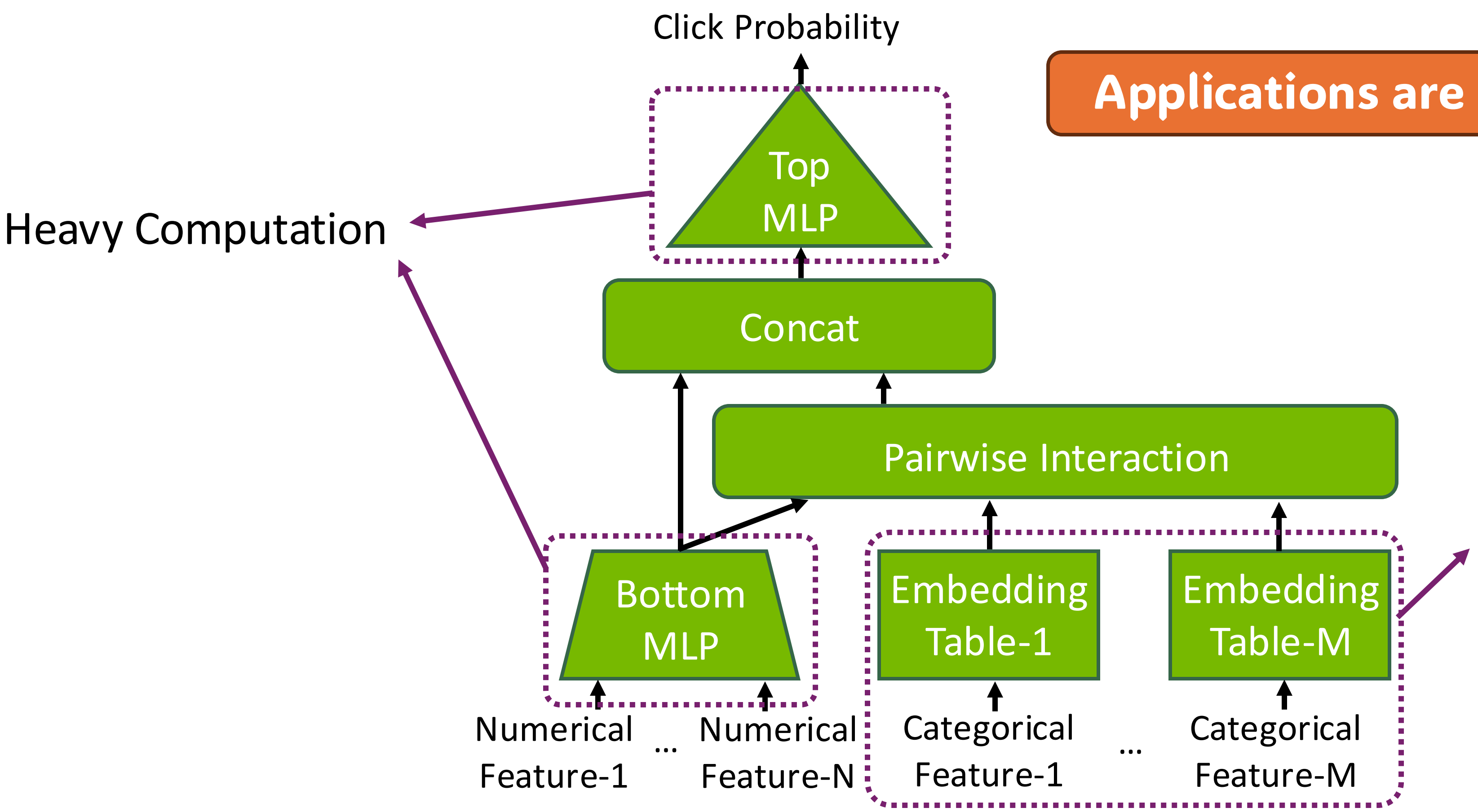


Recommendation System

- Huge embedding tables **far beyond the GPU's memory.**
- Irregular Access.



Recommendation System

Applications are more than just Computation!

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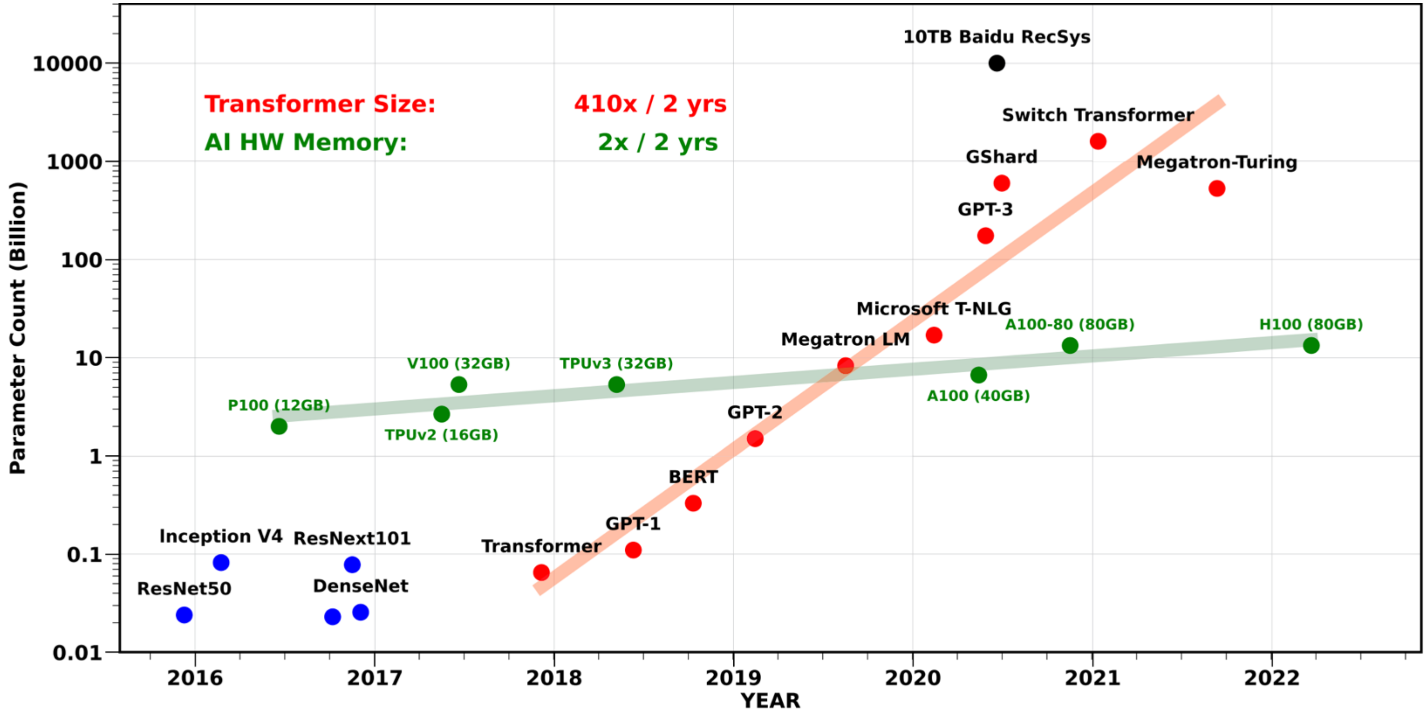

AI and Memory Wall[1]

GPUs are increasingly constrained by the memory wall

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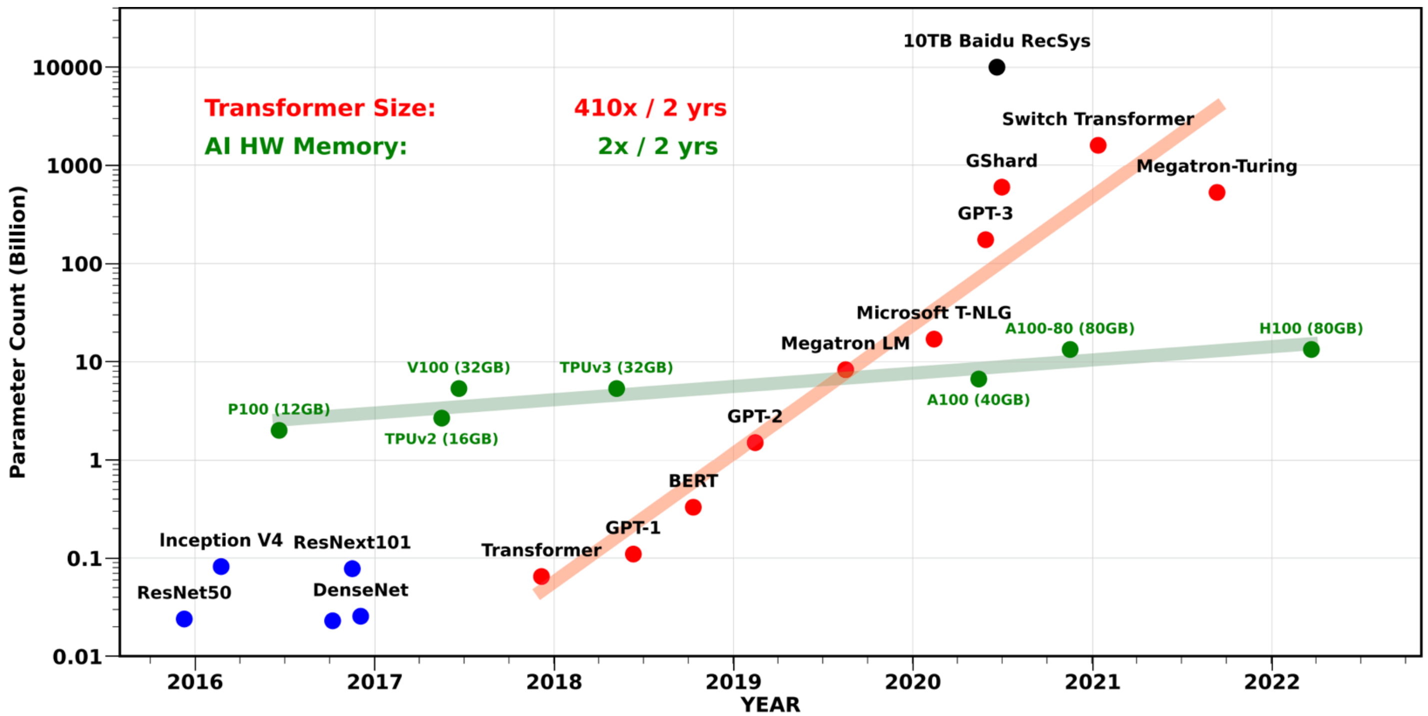

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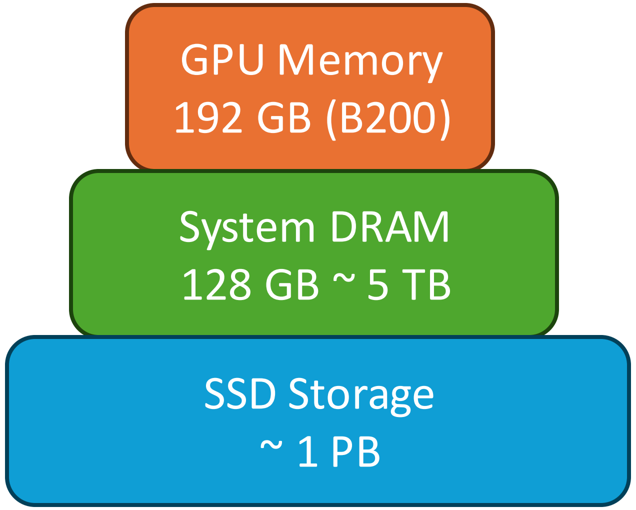

Hierarchical memory in modern computing systems

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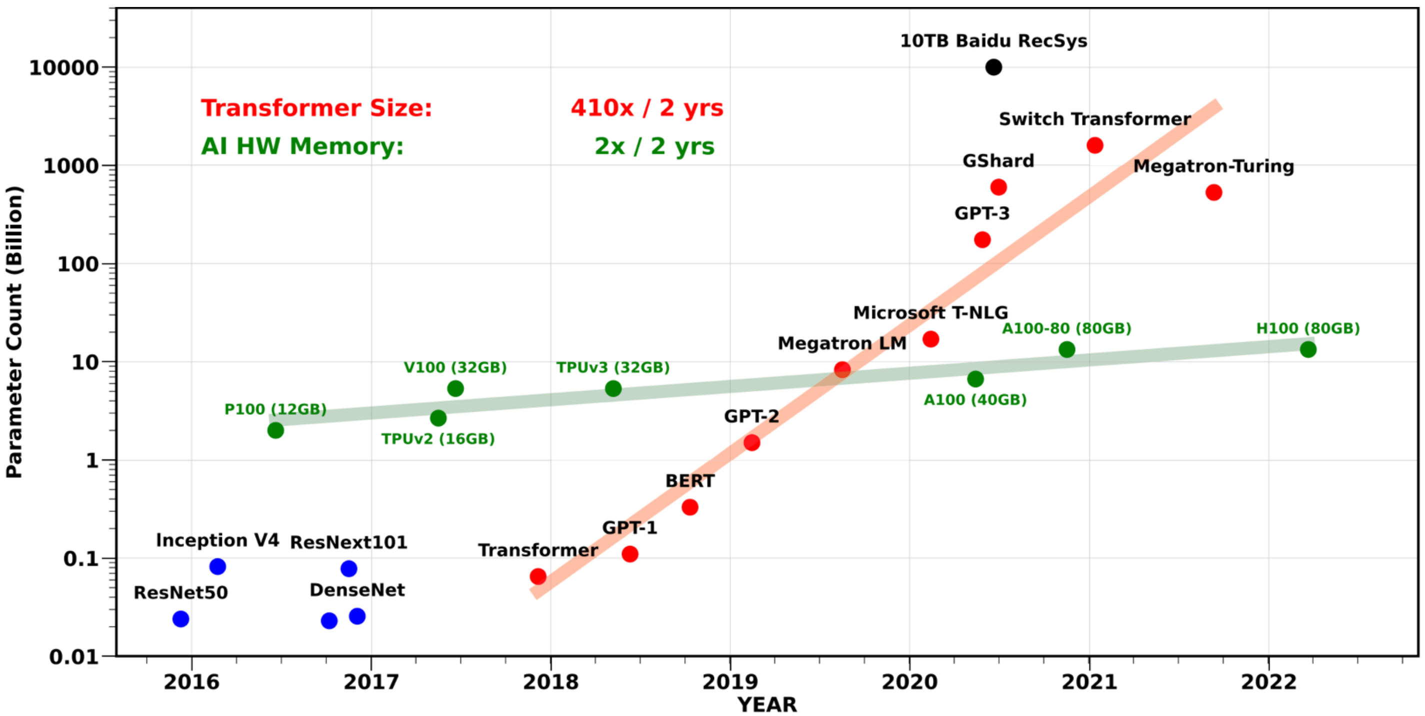

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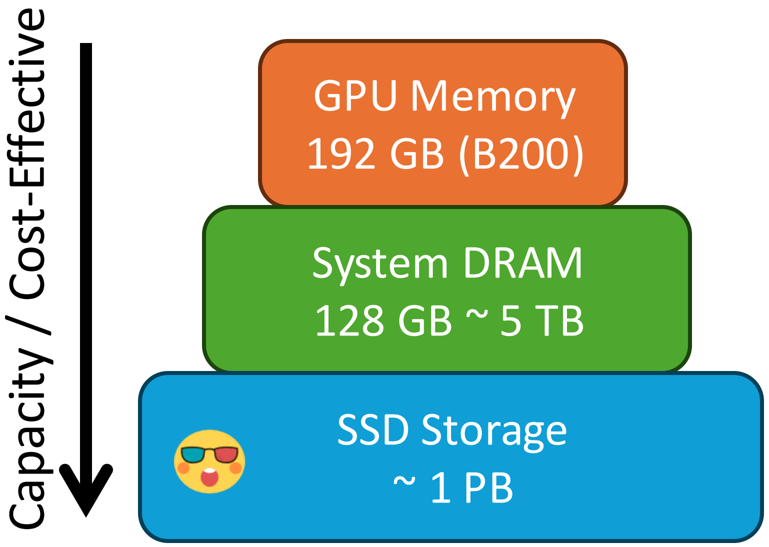

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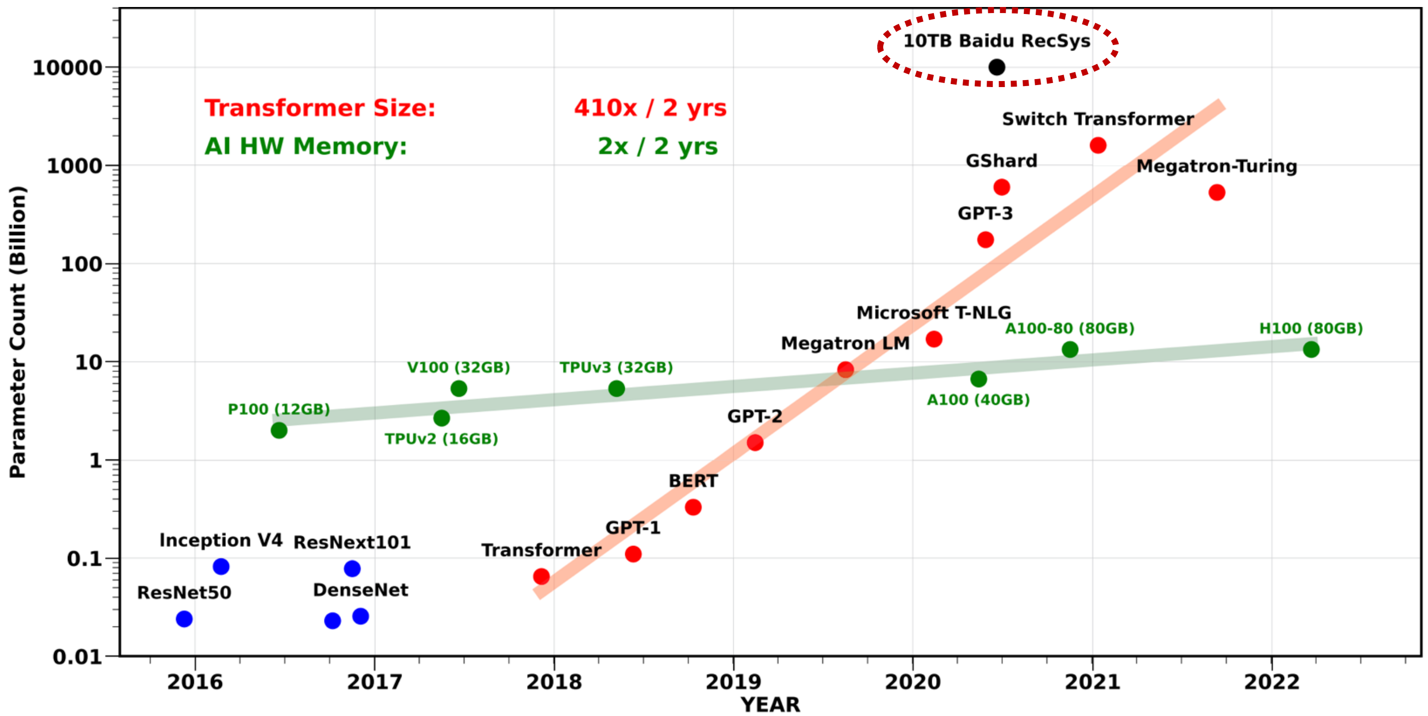

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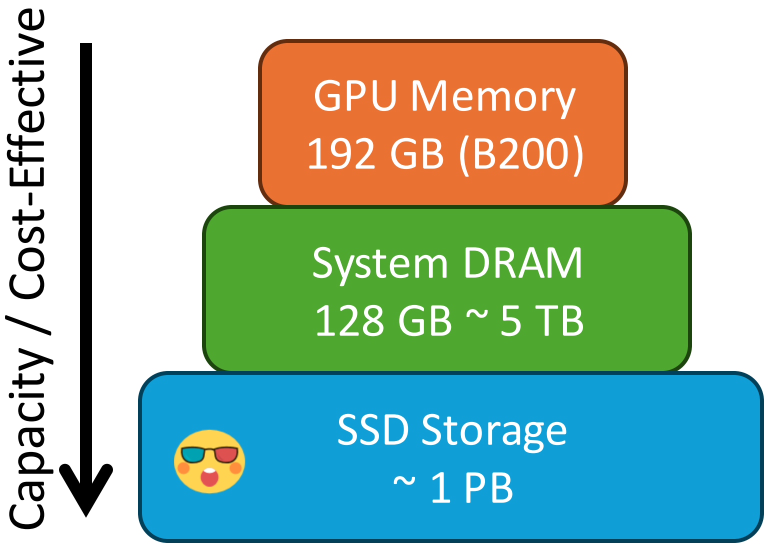

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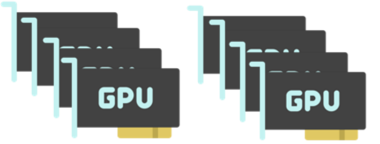
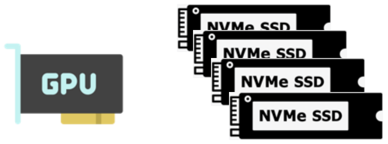
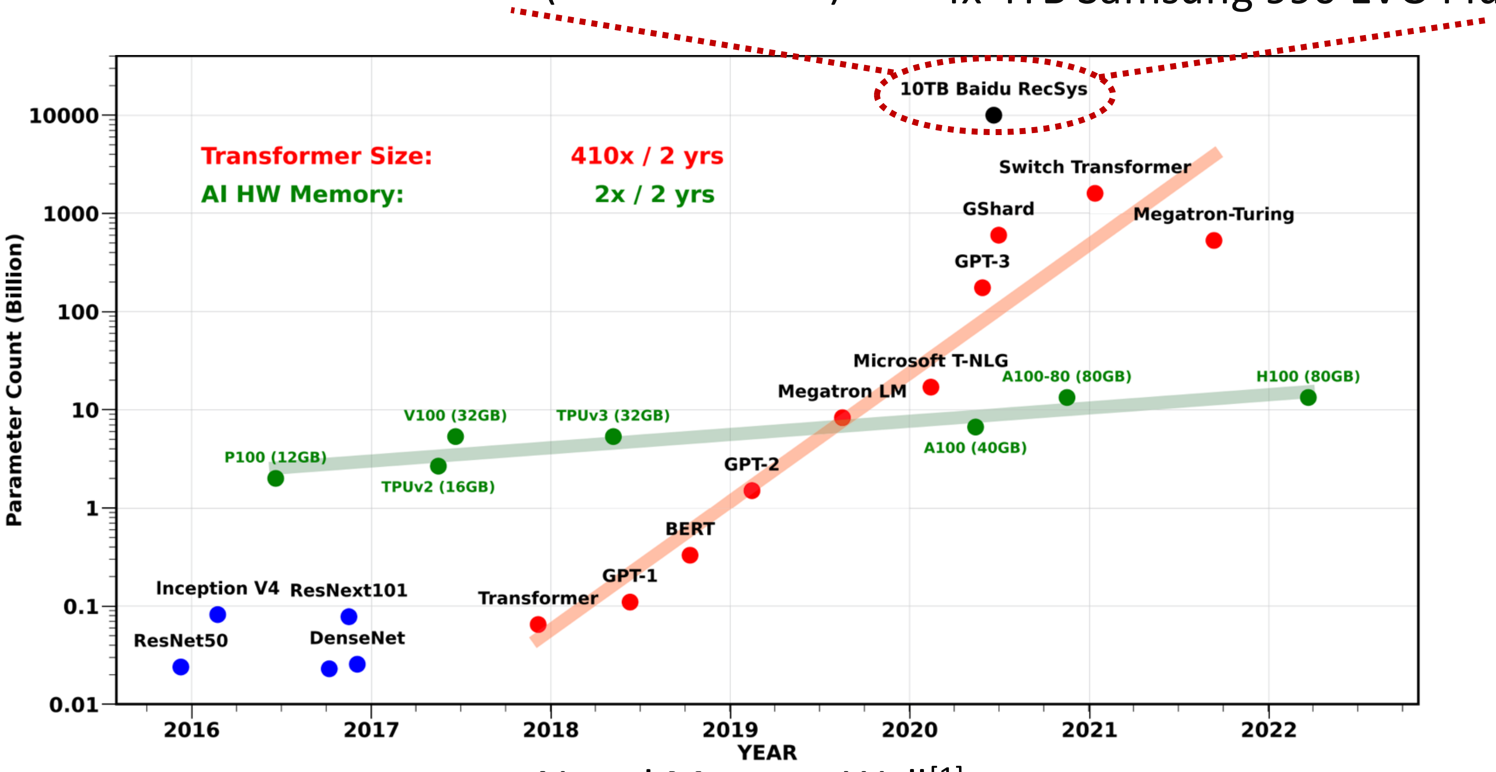


NVIDIA DGX B200
(8x B200 GPUs)

V.S.



NVIDIA B200 +
4x 4TB Samsung 990 EVO Plus



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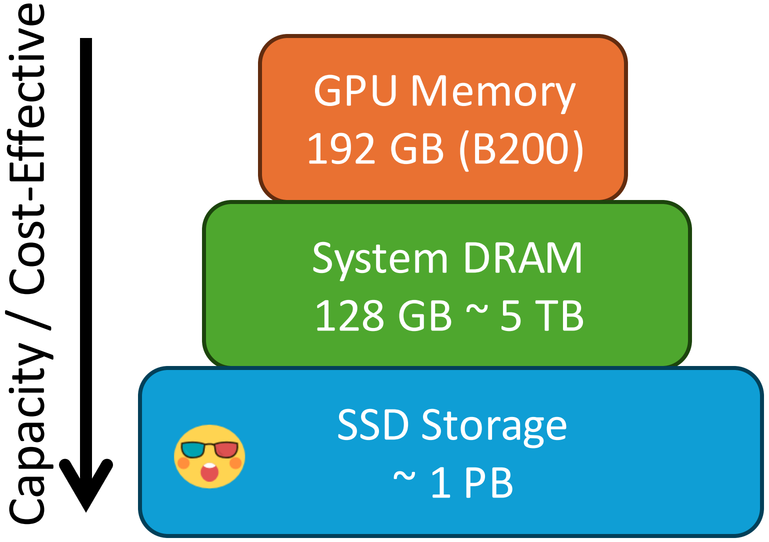

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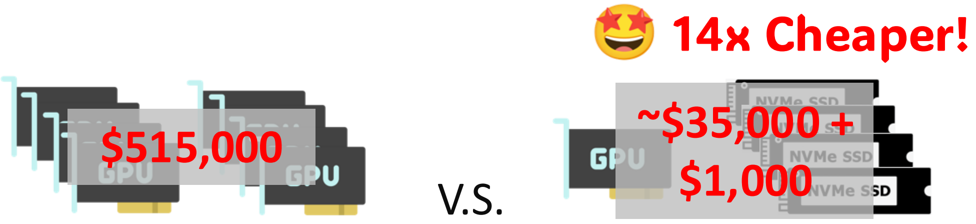

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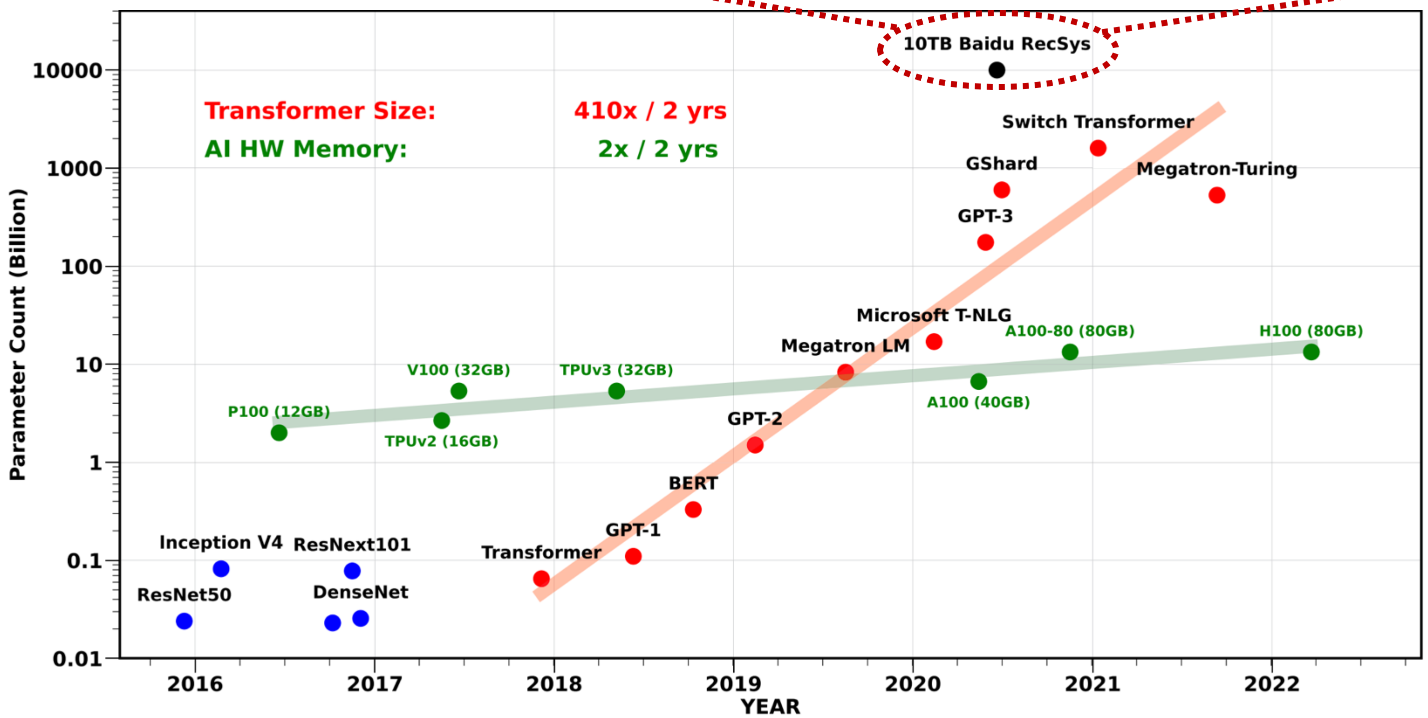

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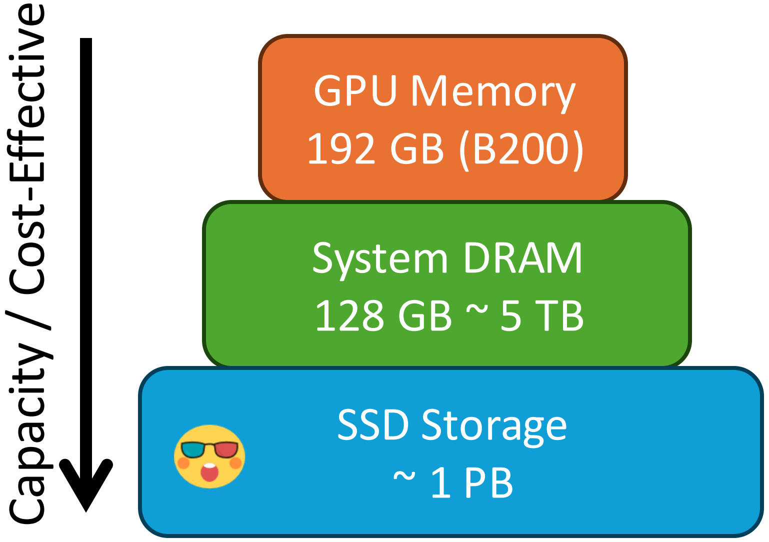

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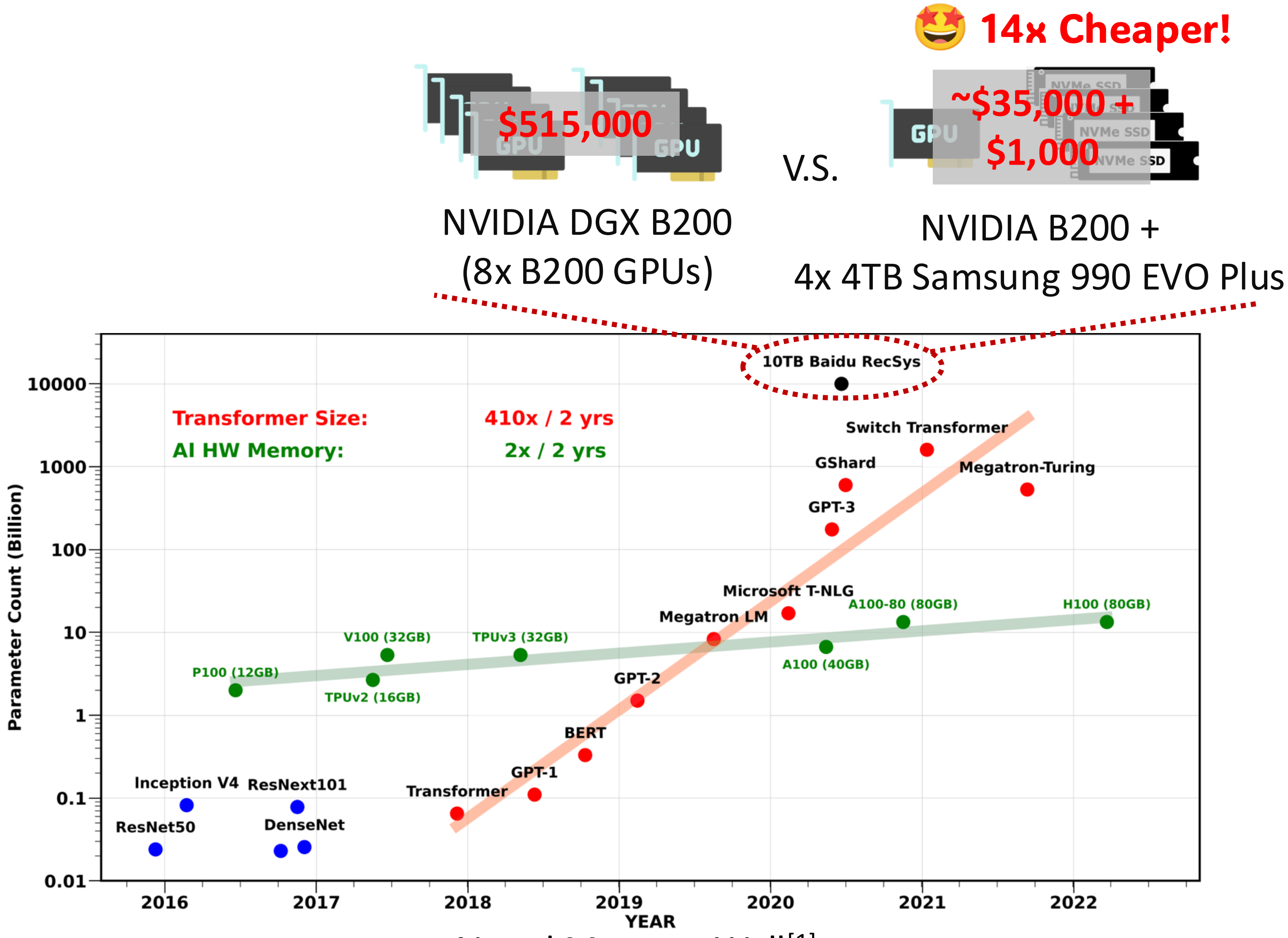

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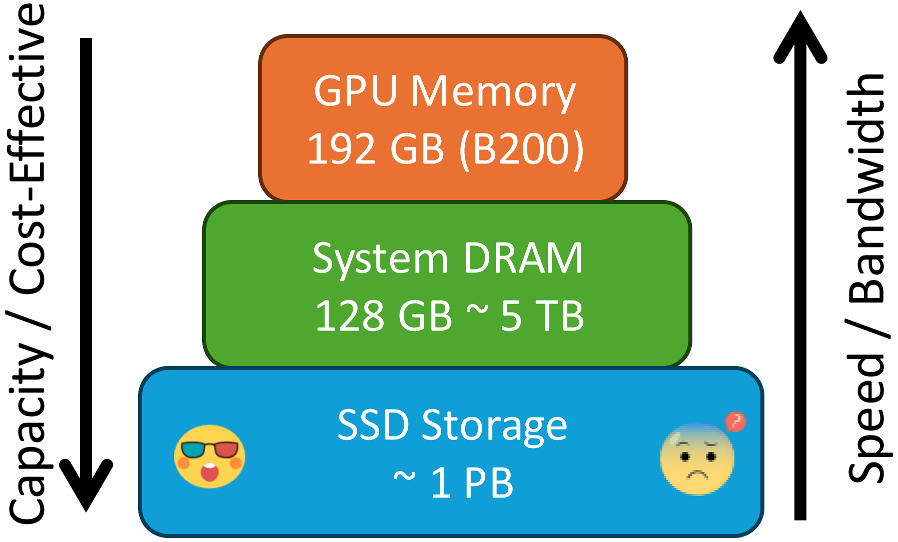

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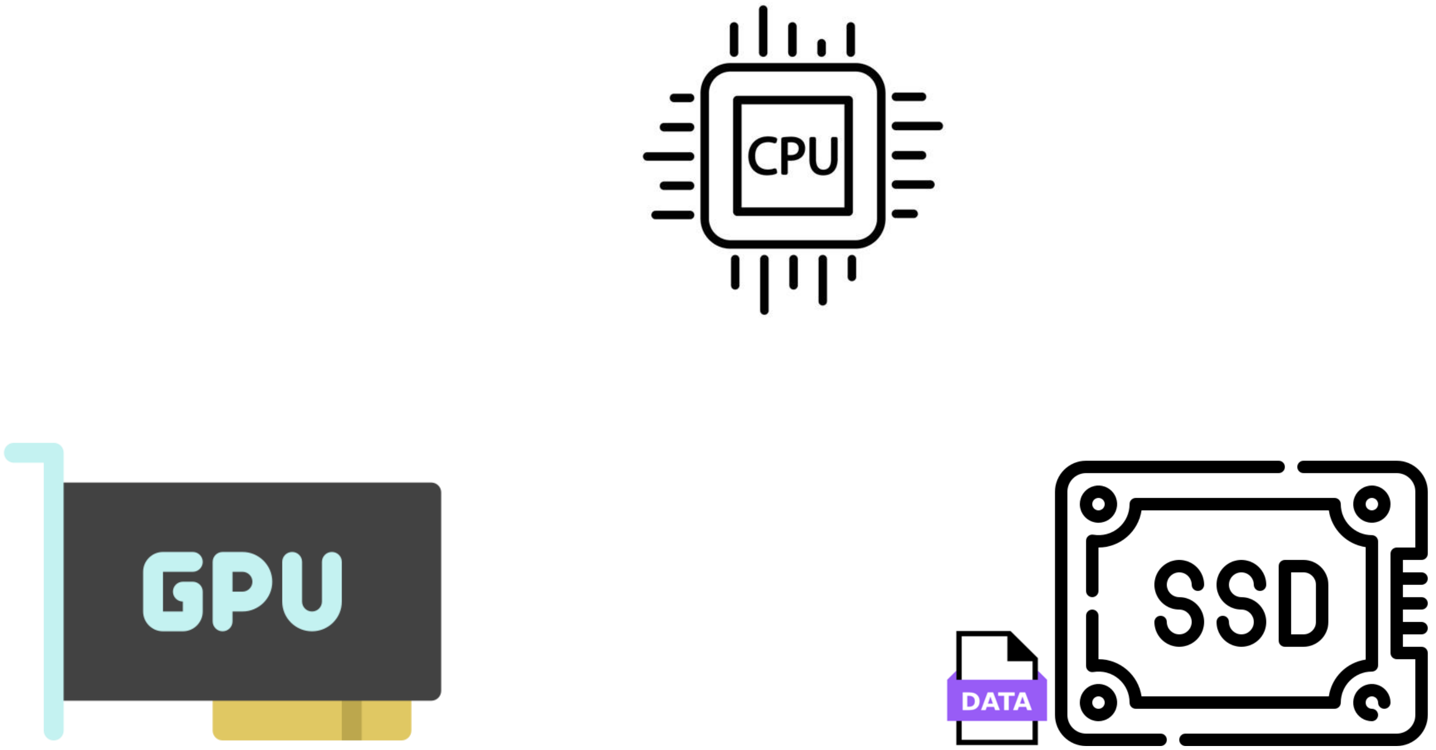
BaM[1] (A GPU-Centric Storage Access Model)



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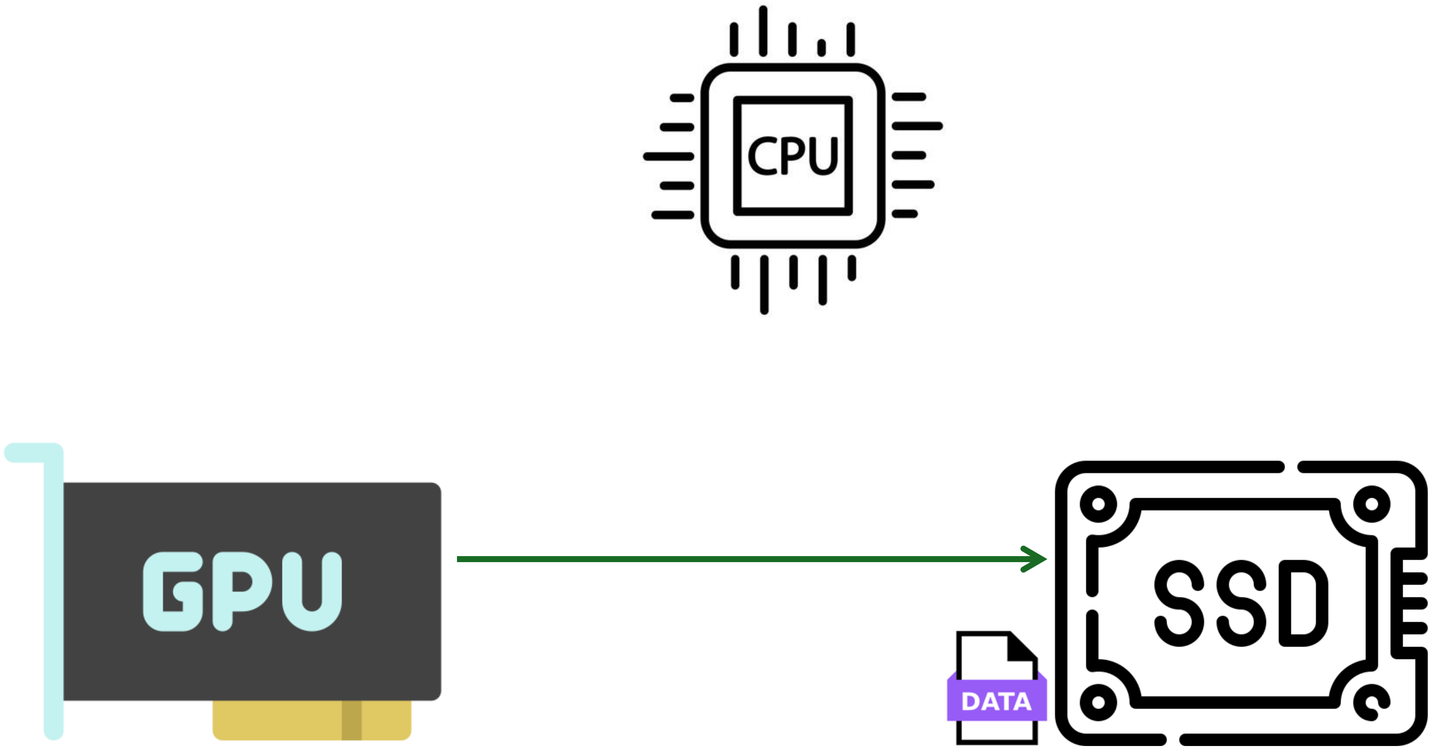

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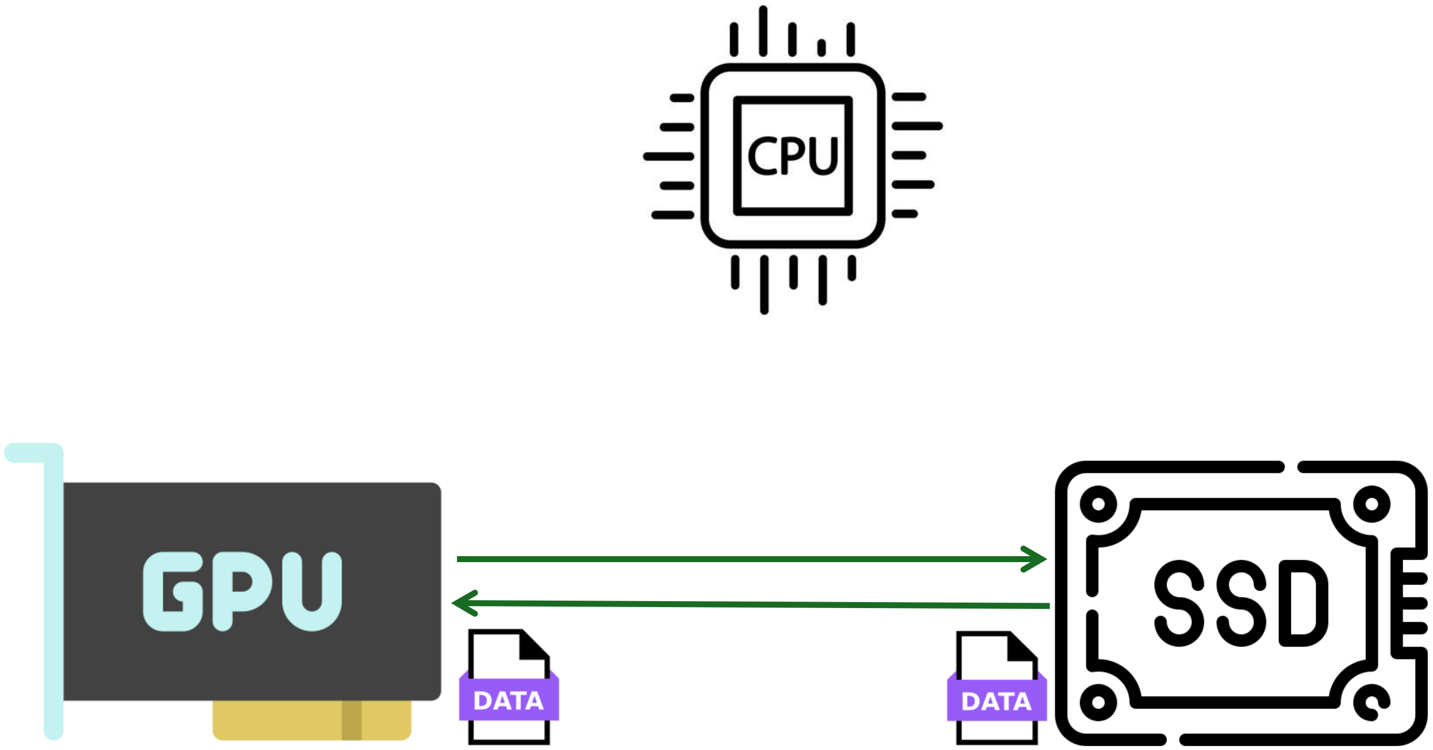

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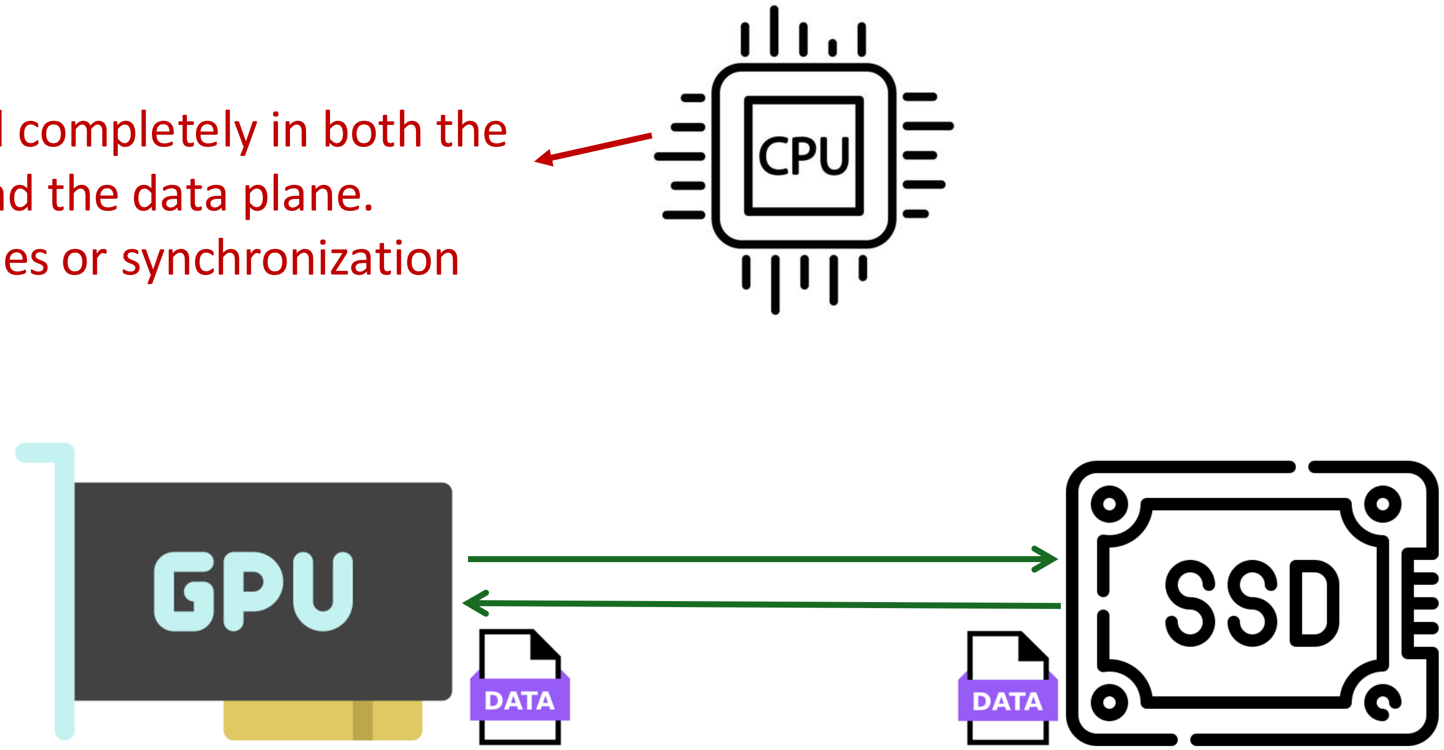
CPU is bypassed completely in both the control plane and the data plane.

- ➢ No extra copies or synchronization overheads



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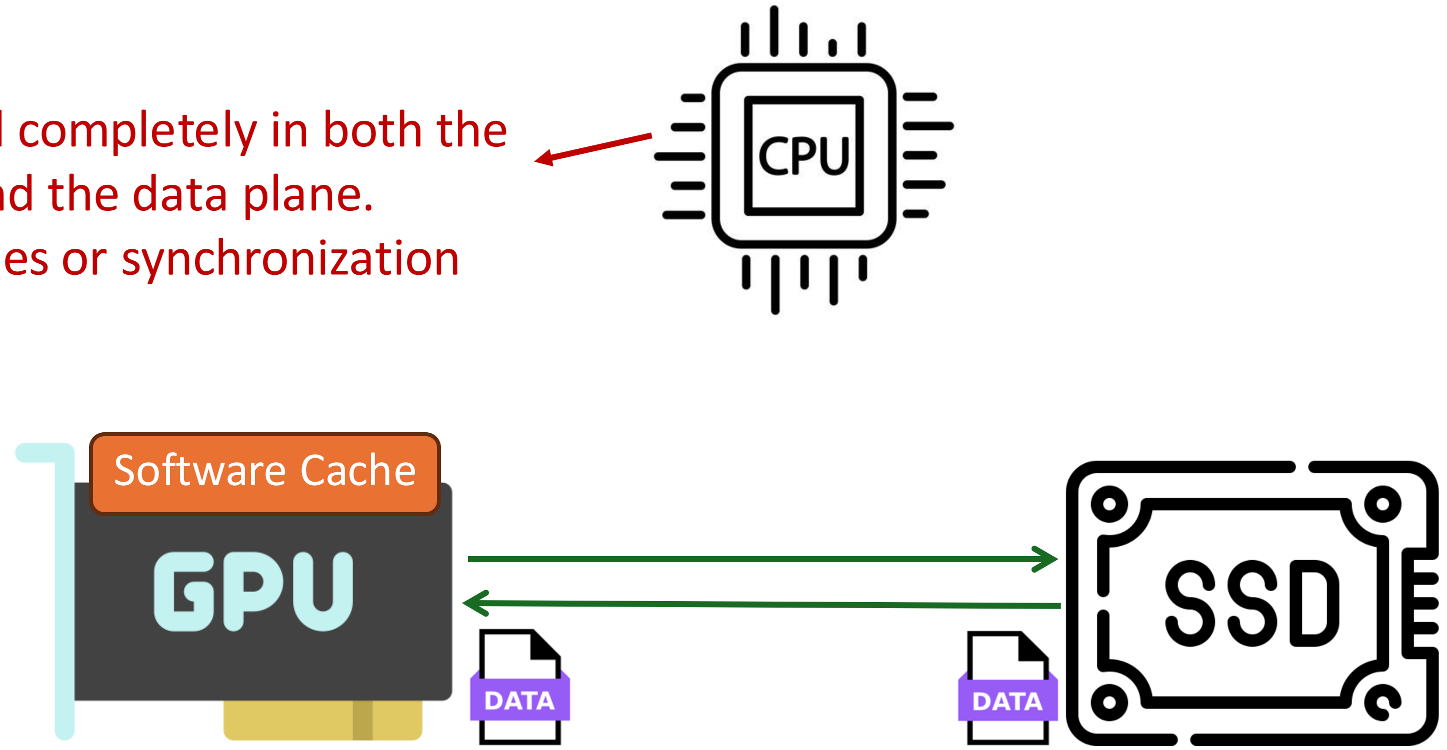

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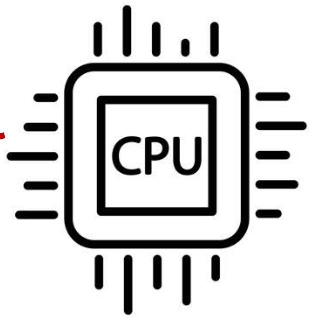
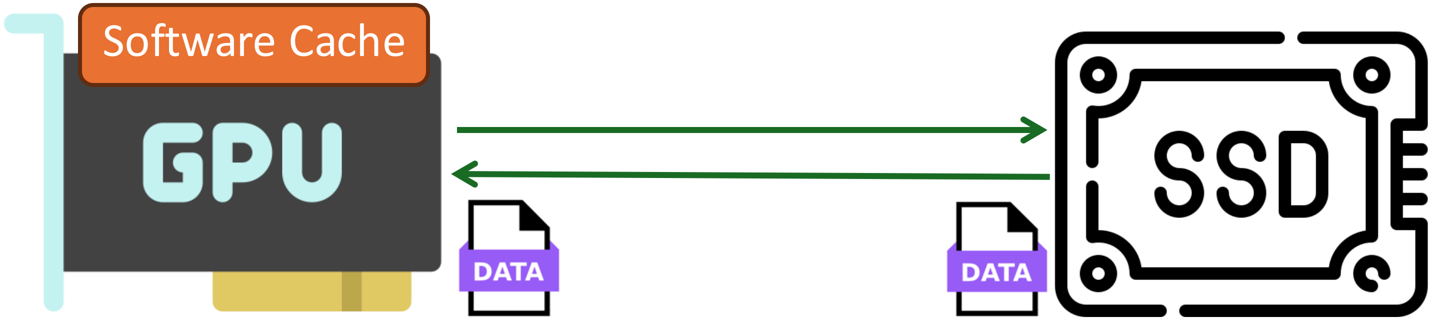


Can we further improve the GPU-centric storage access model?



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Programming Models for GPU-Centric I/O

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Synchronous I/O Model
(BaM)

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Programming Models for GPU-Centric I/O

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Async I/O enables overlapping the slow transfer with other tasks.

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How can we support an async GPU-centric storage access model efficiently?

Programming Models for GPU-Centric I/O

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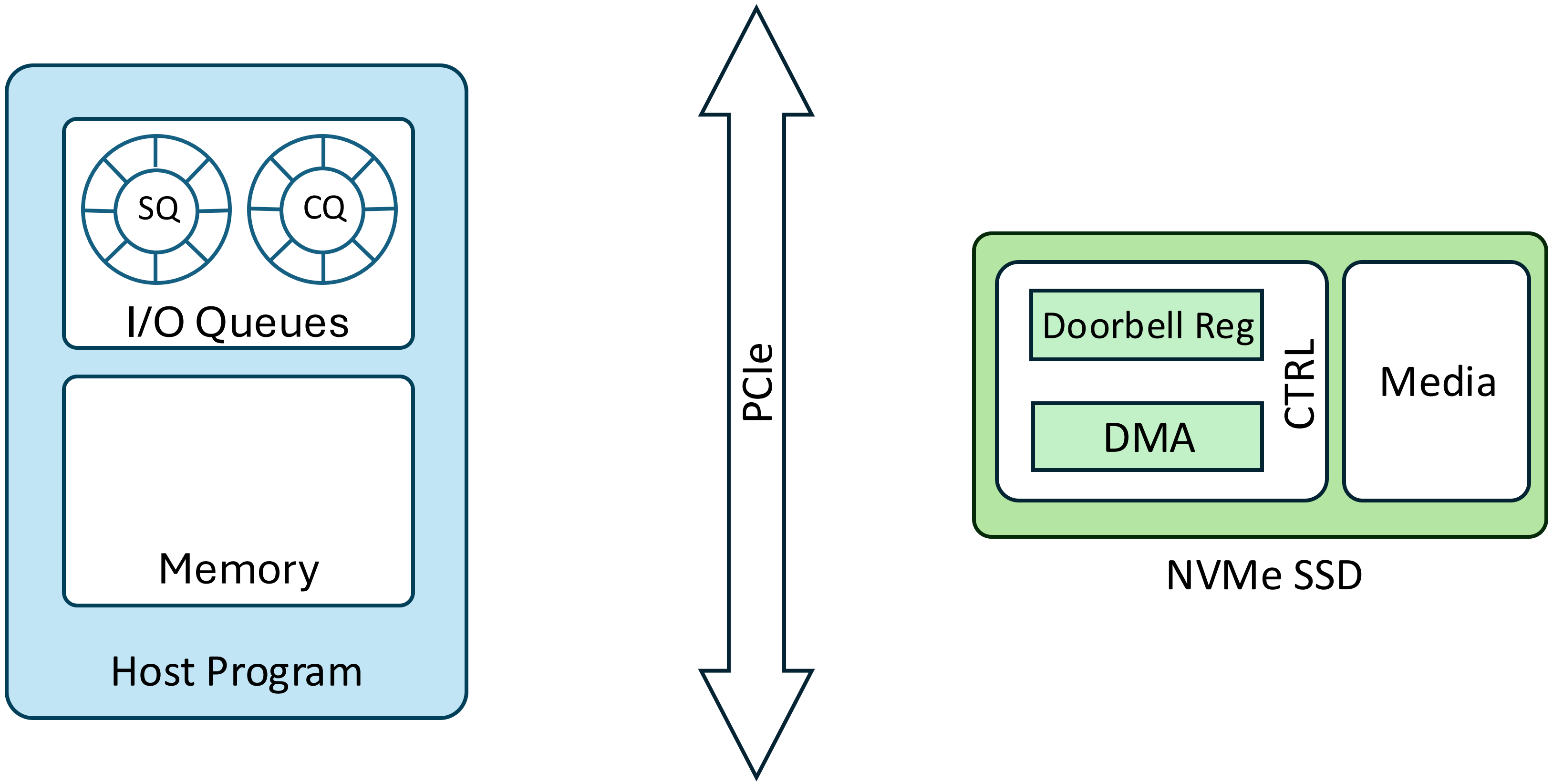
Asynchronous I/O Model

How can we support an async GPU-centric storage access model efficiently?

➢ Use AGILE! (this work)

Background of NVMe Protocol



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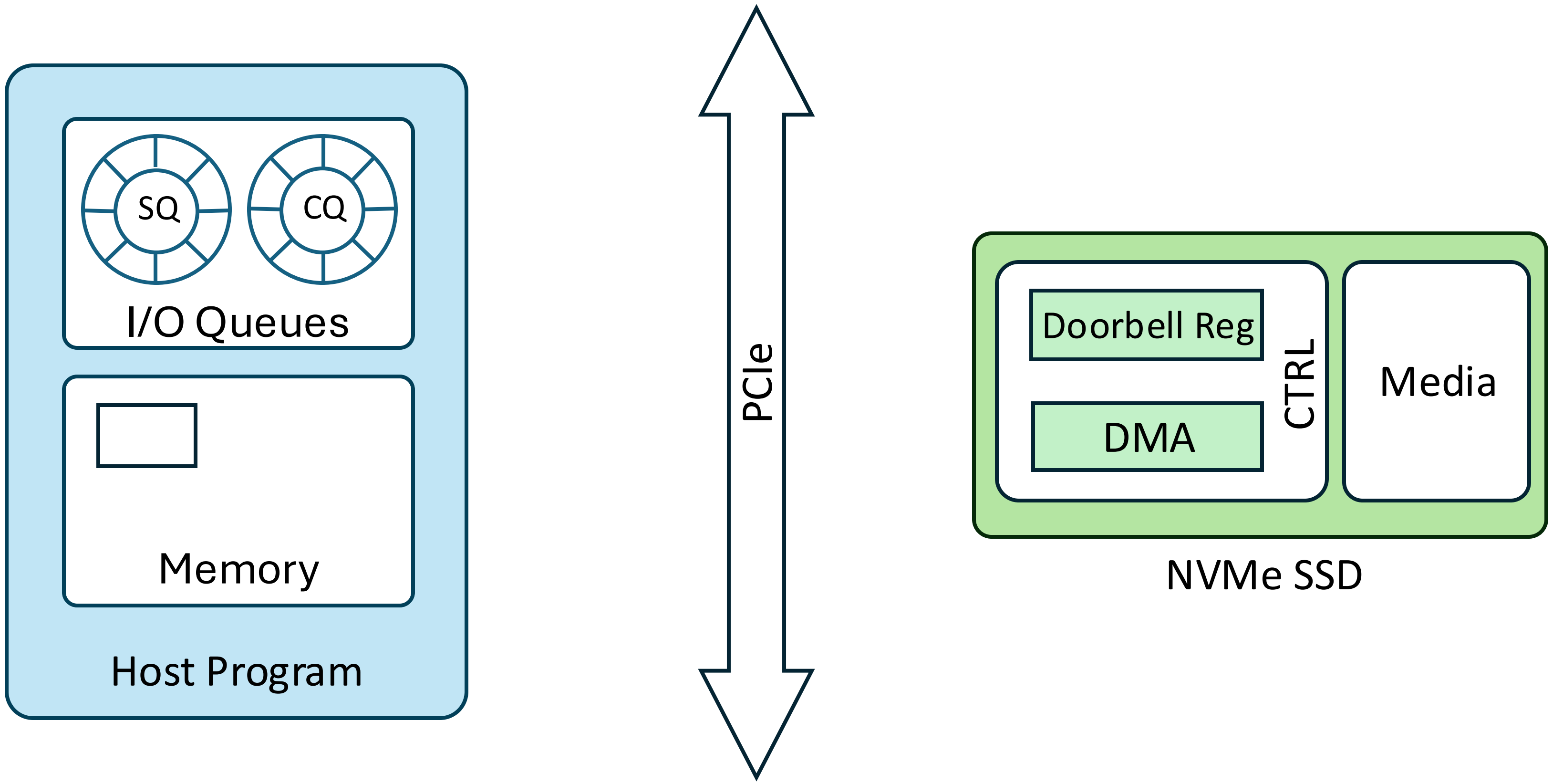

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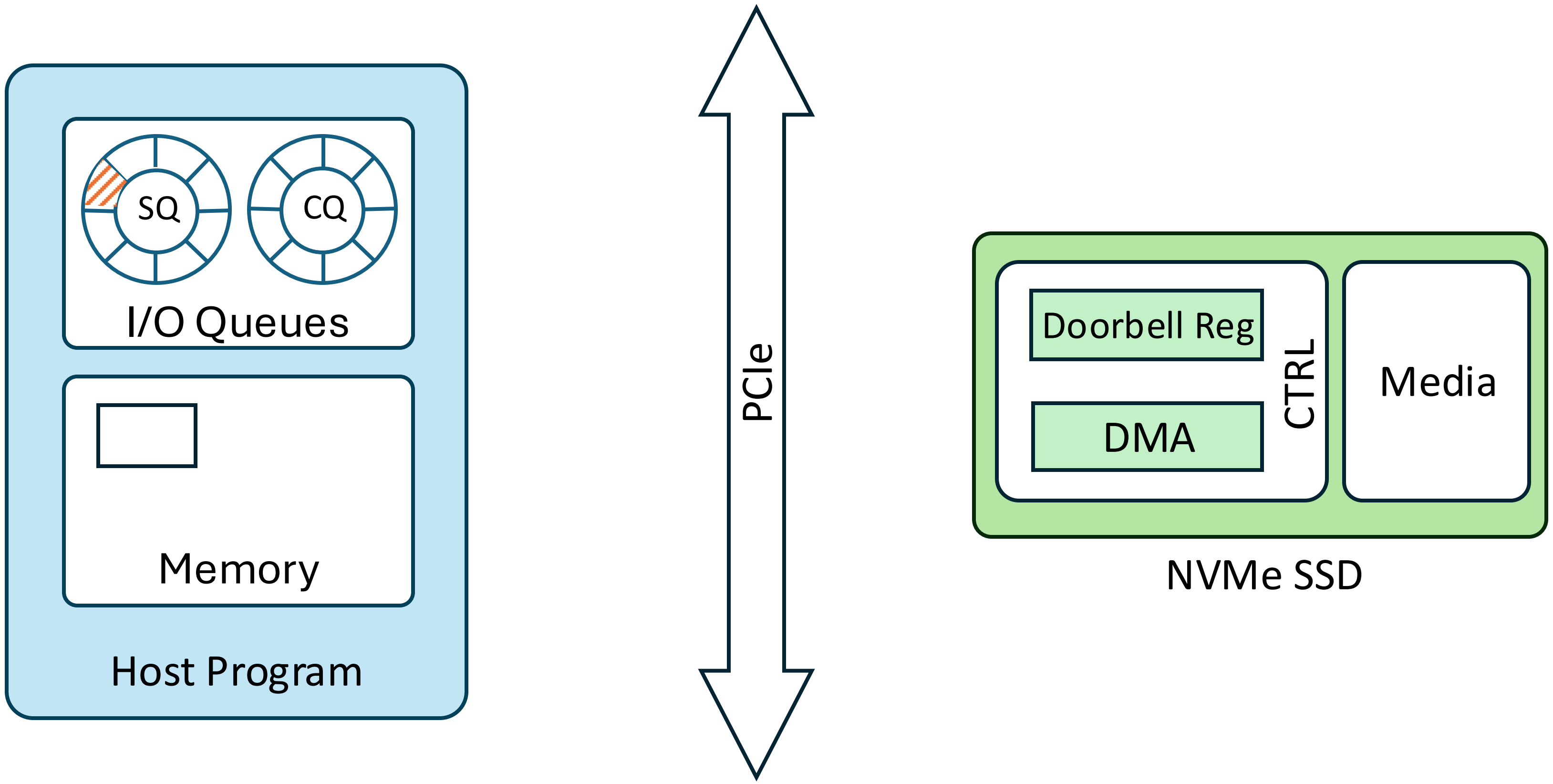

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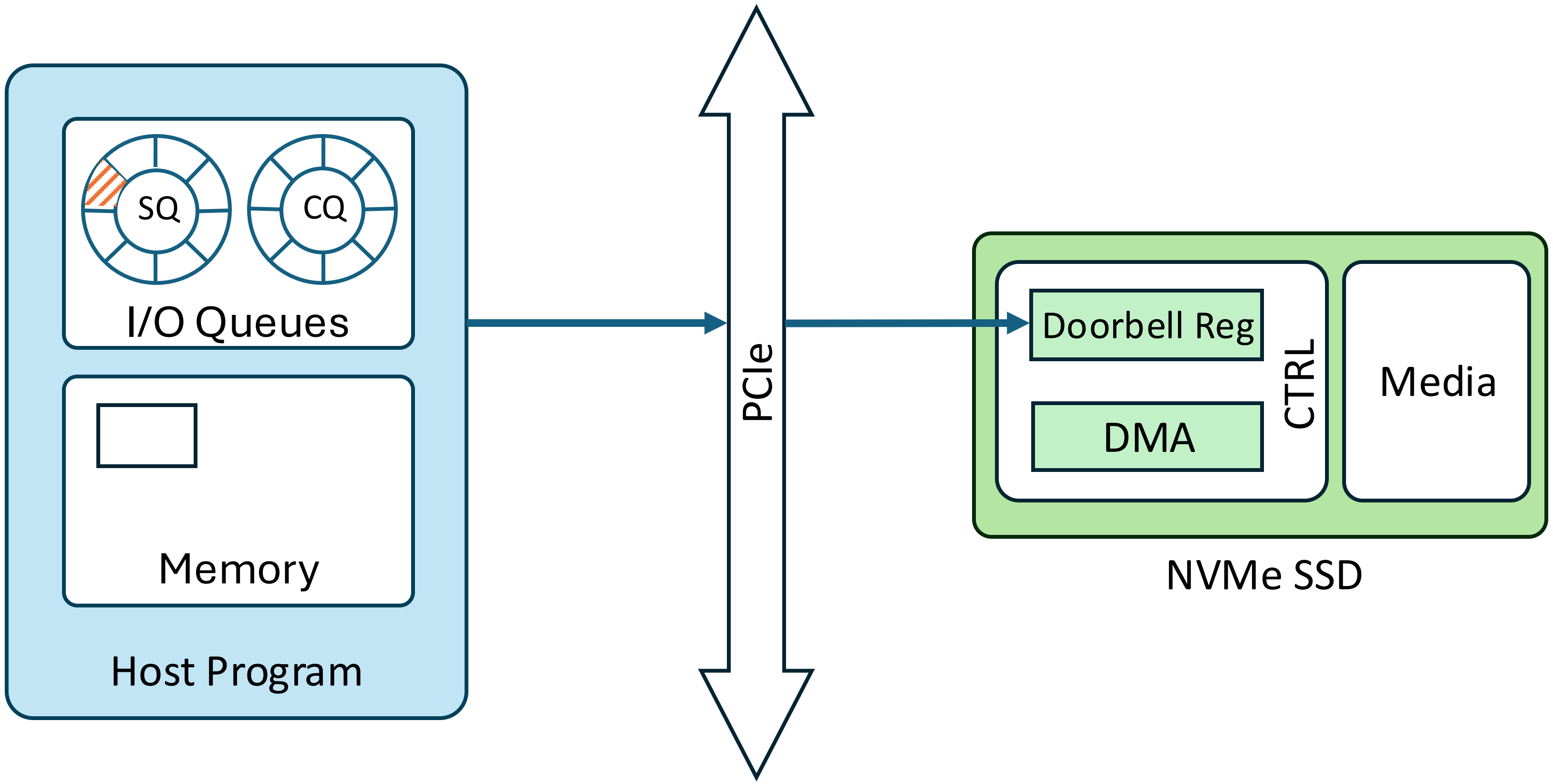

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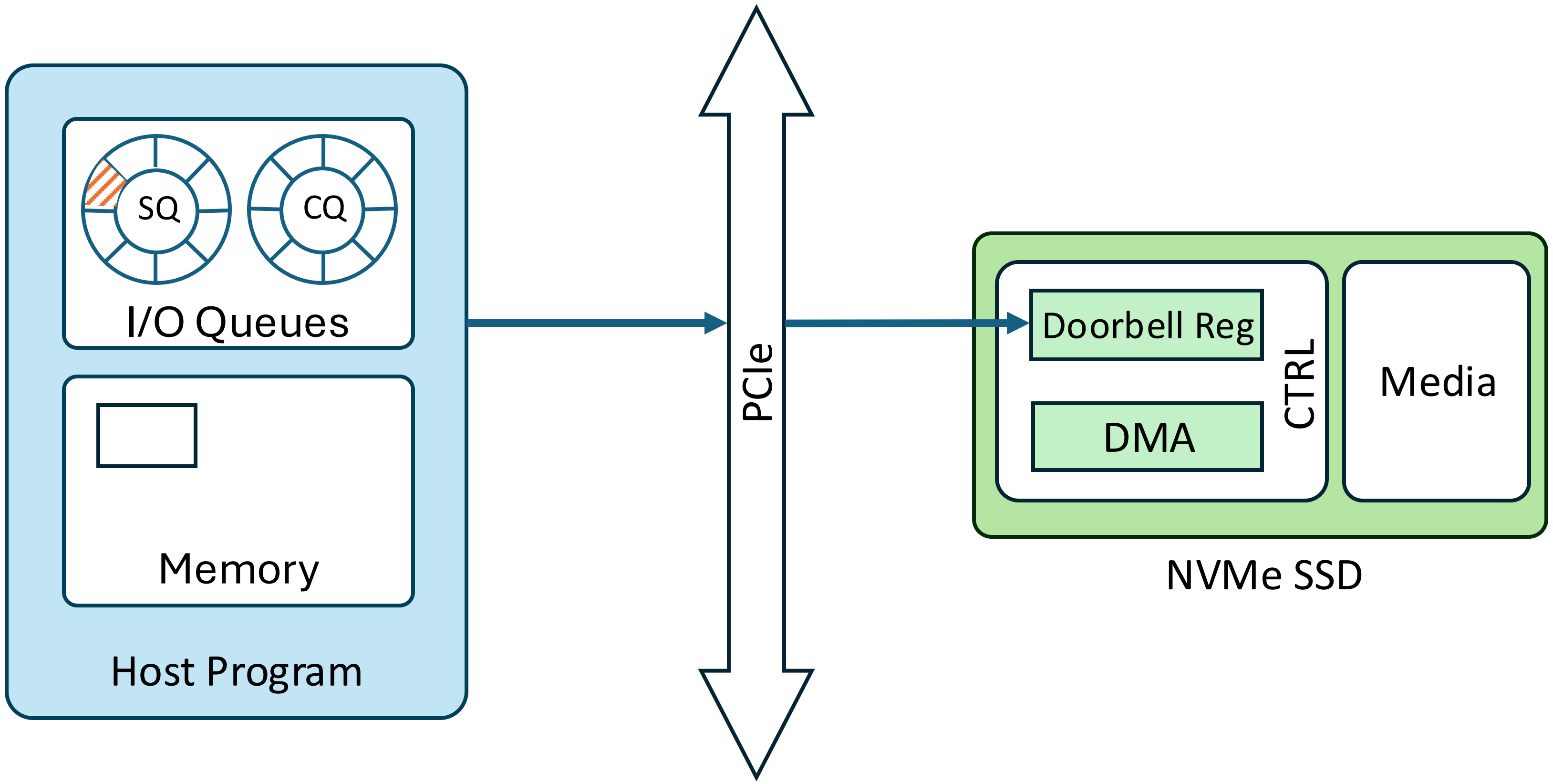

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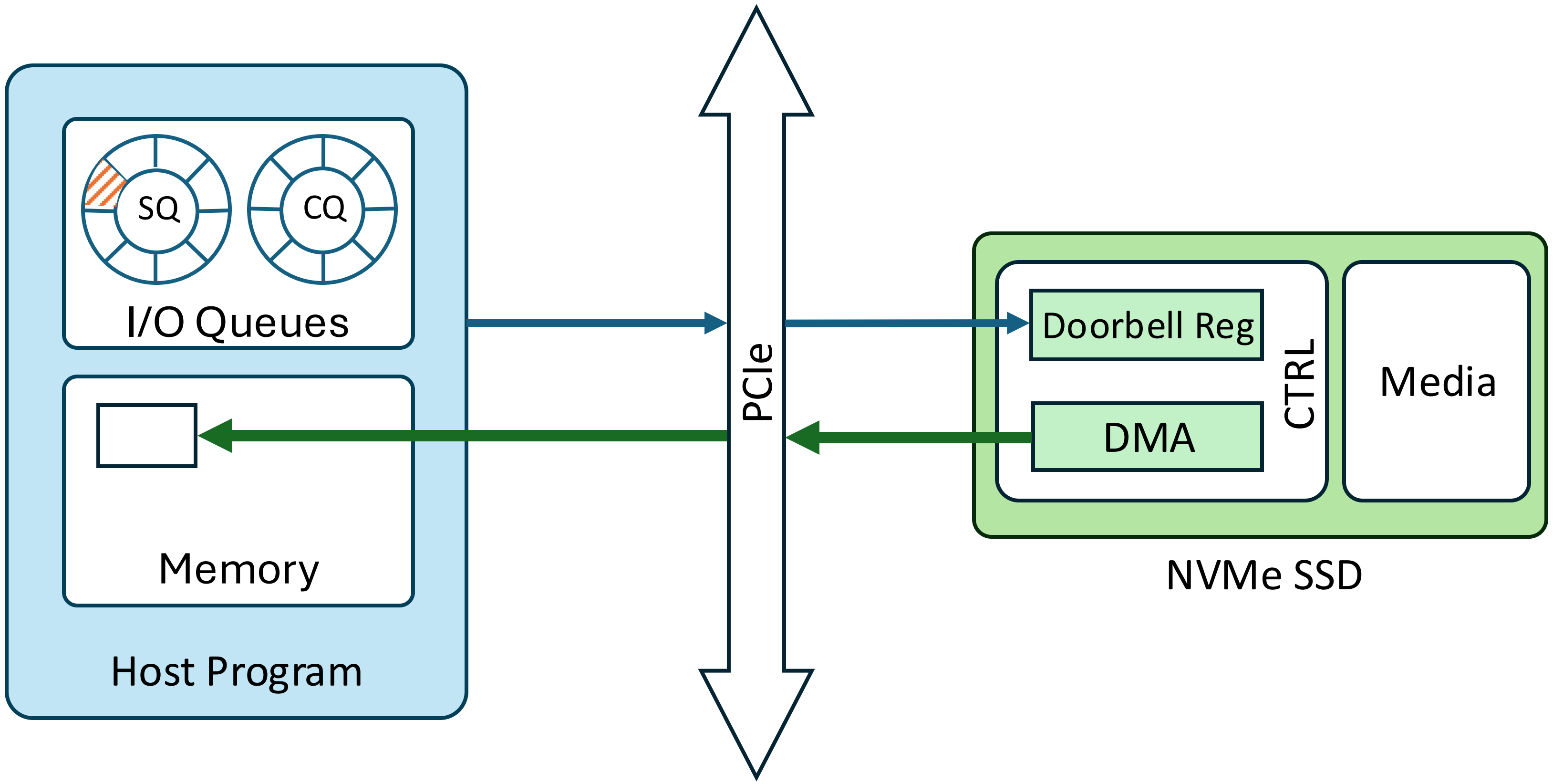

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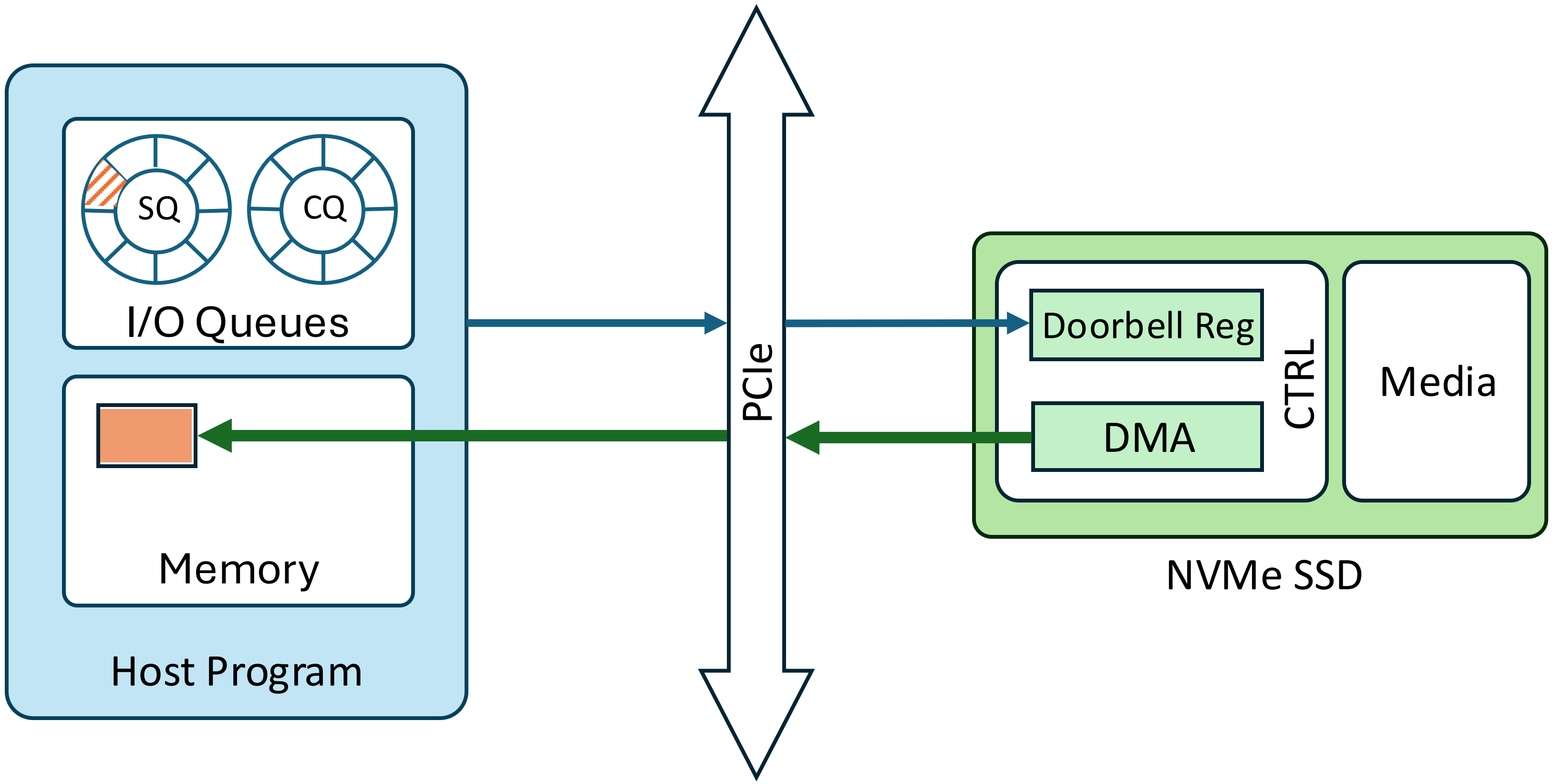

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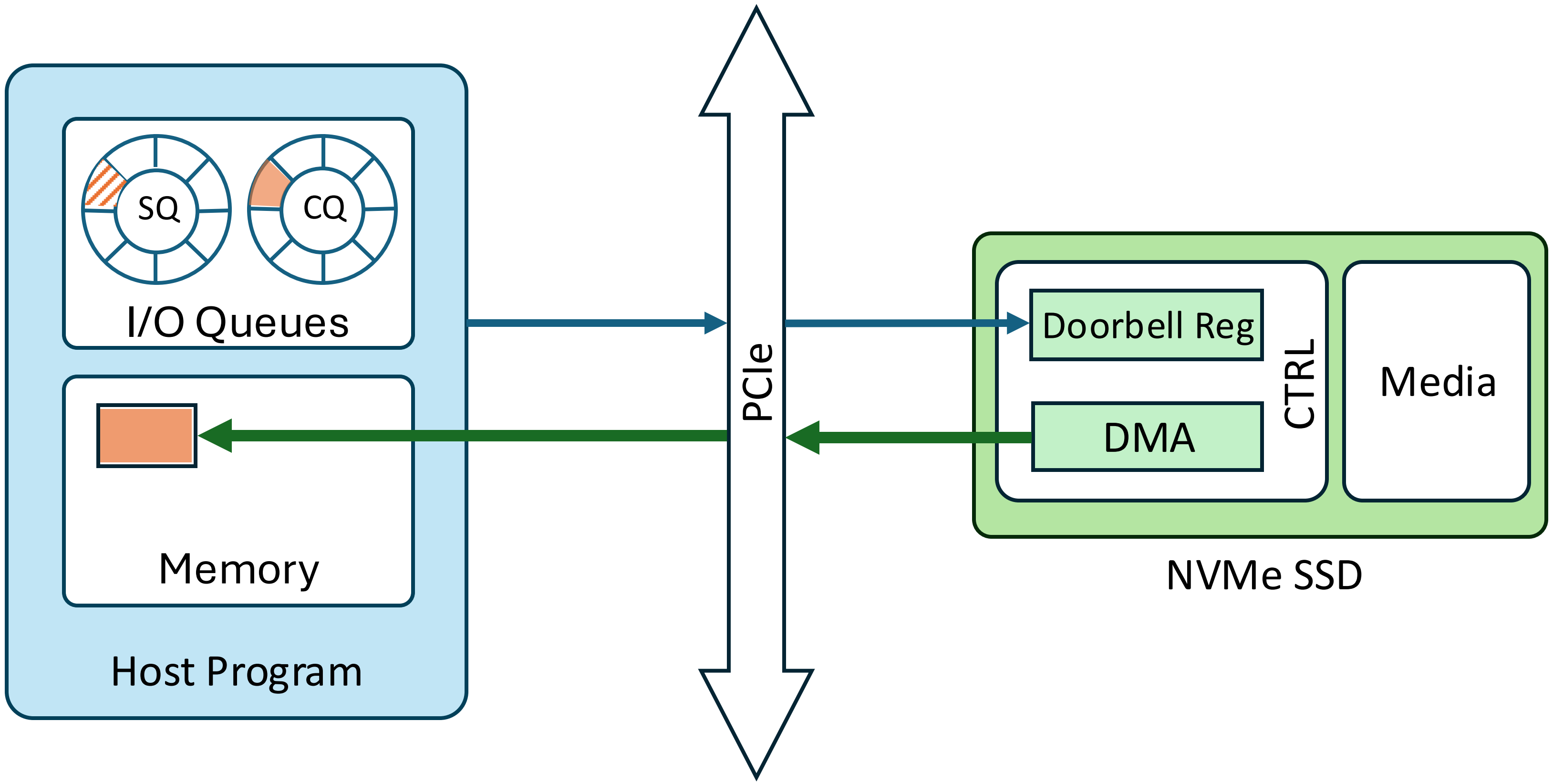

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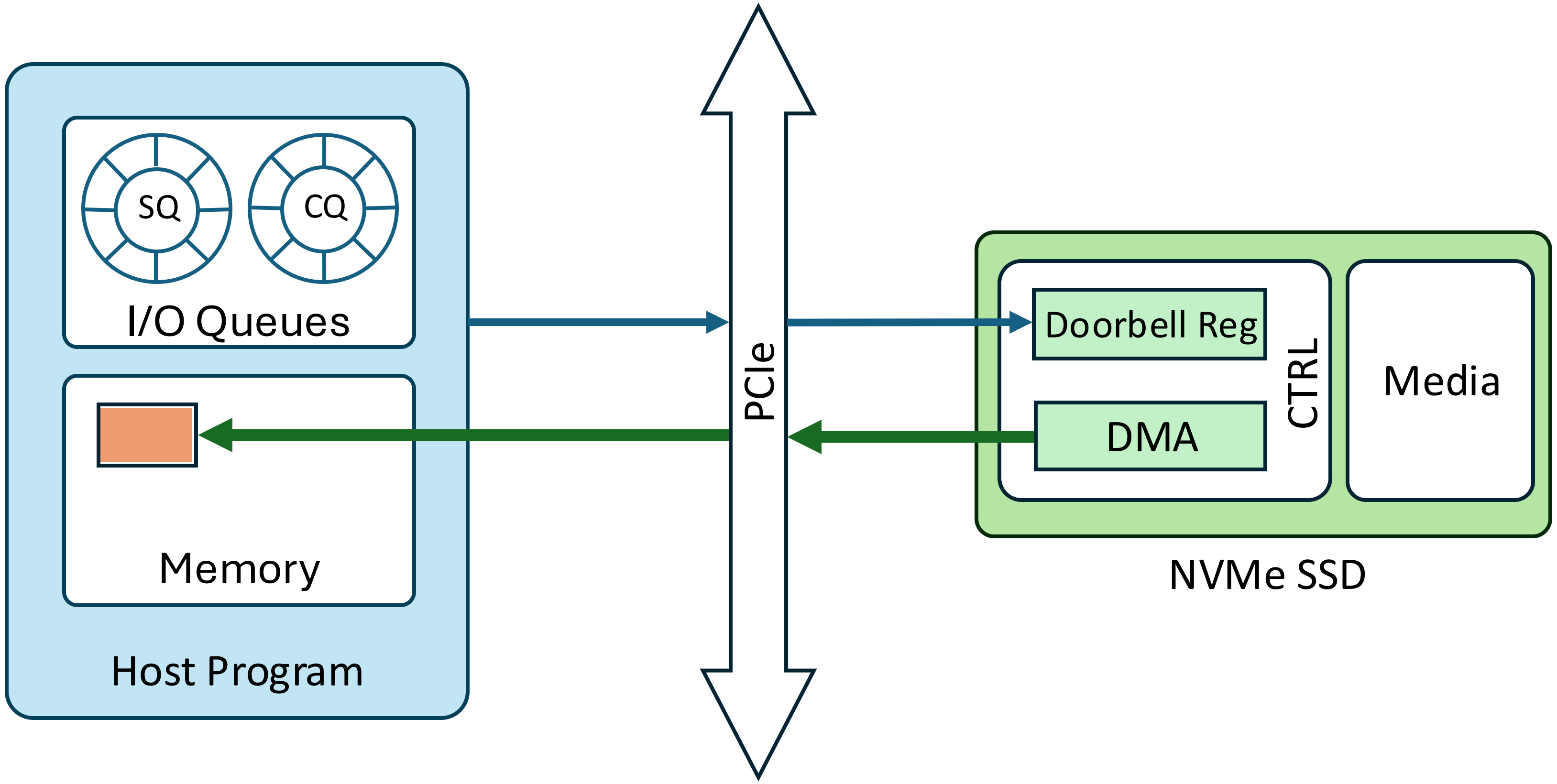

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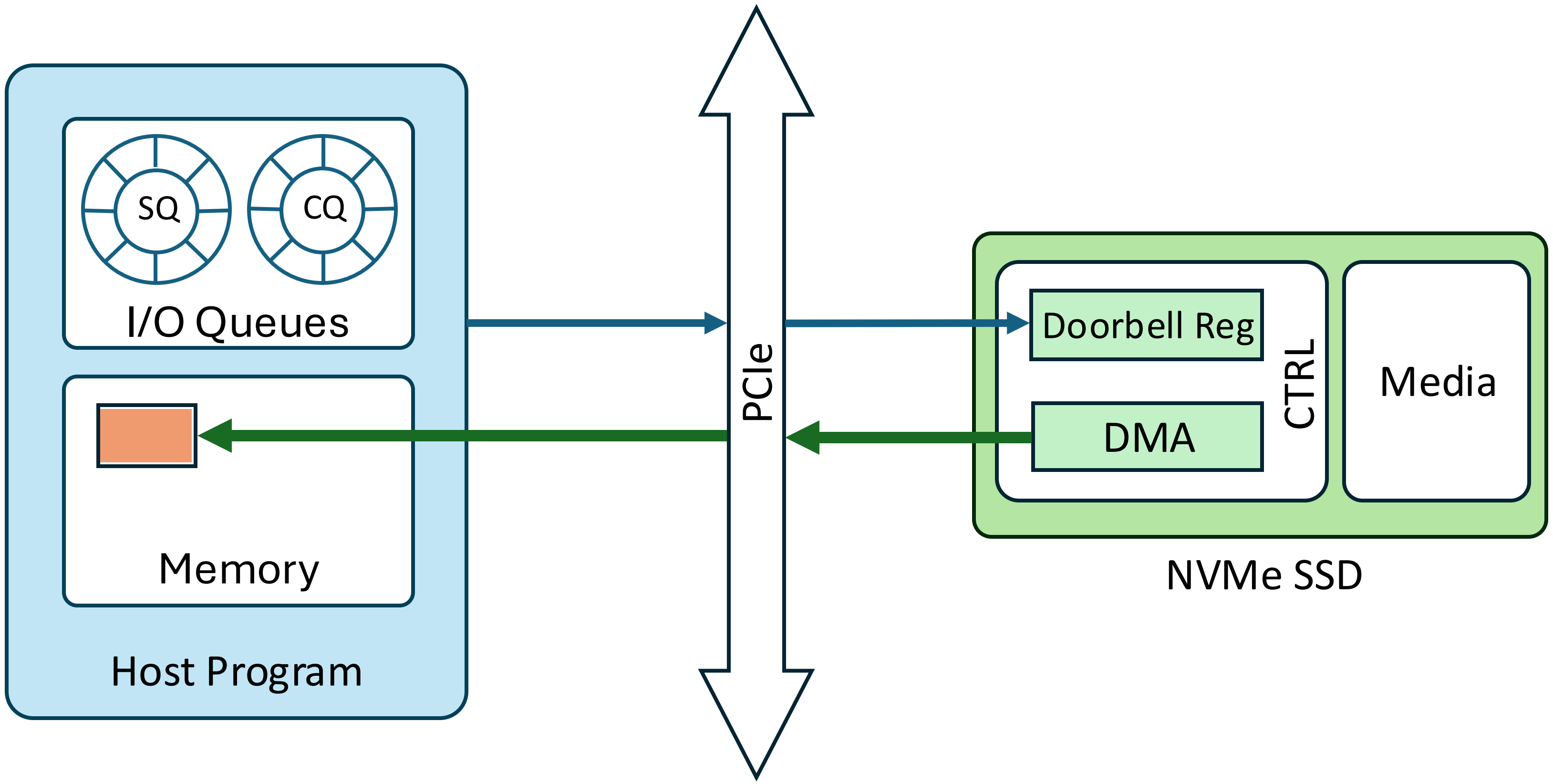

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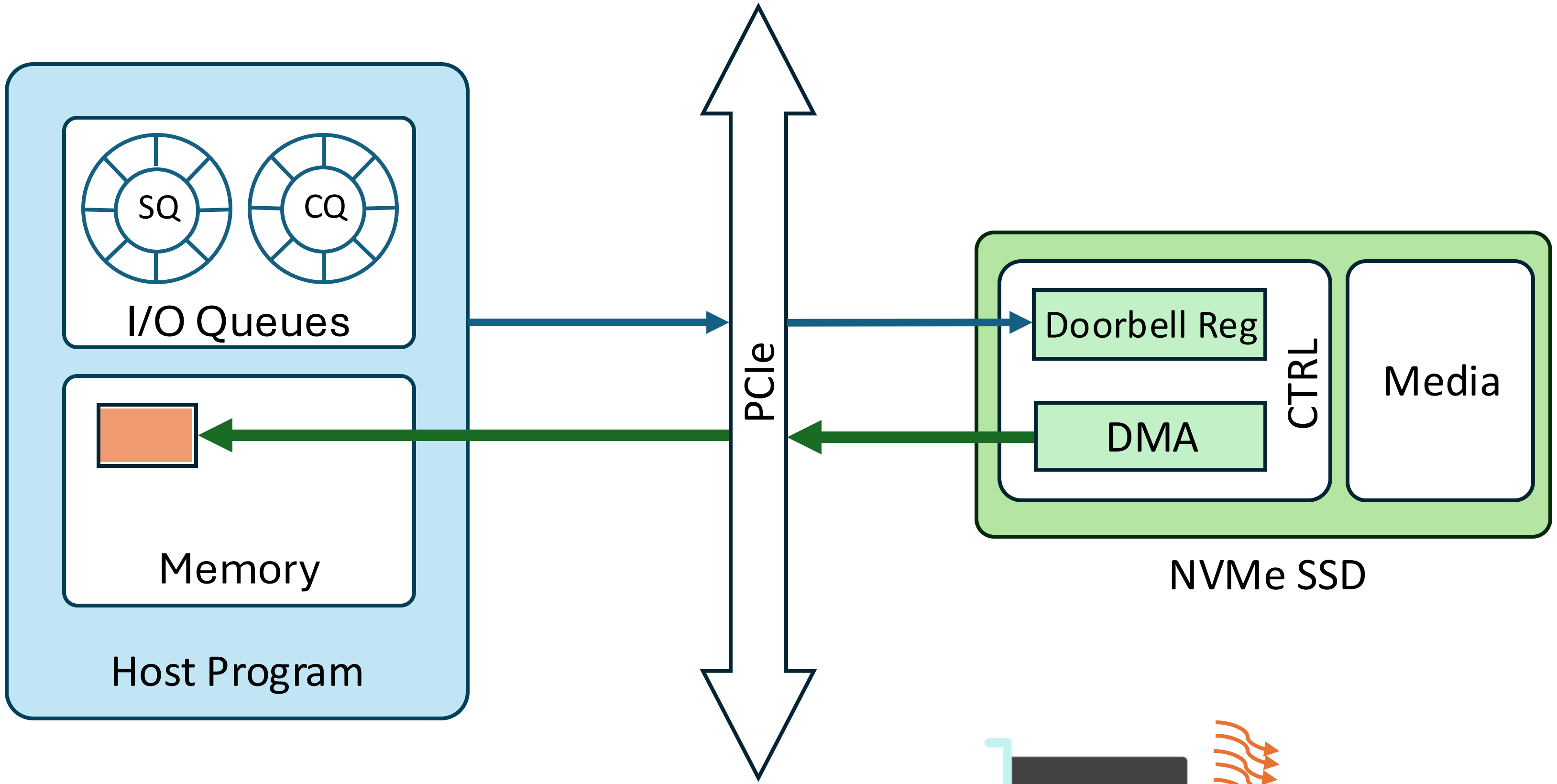

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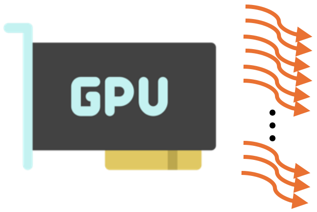
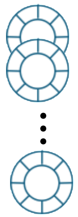
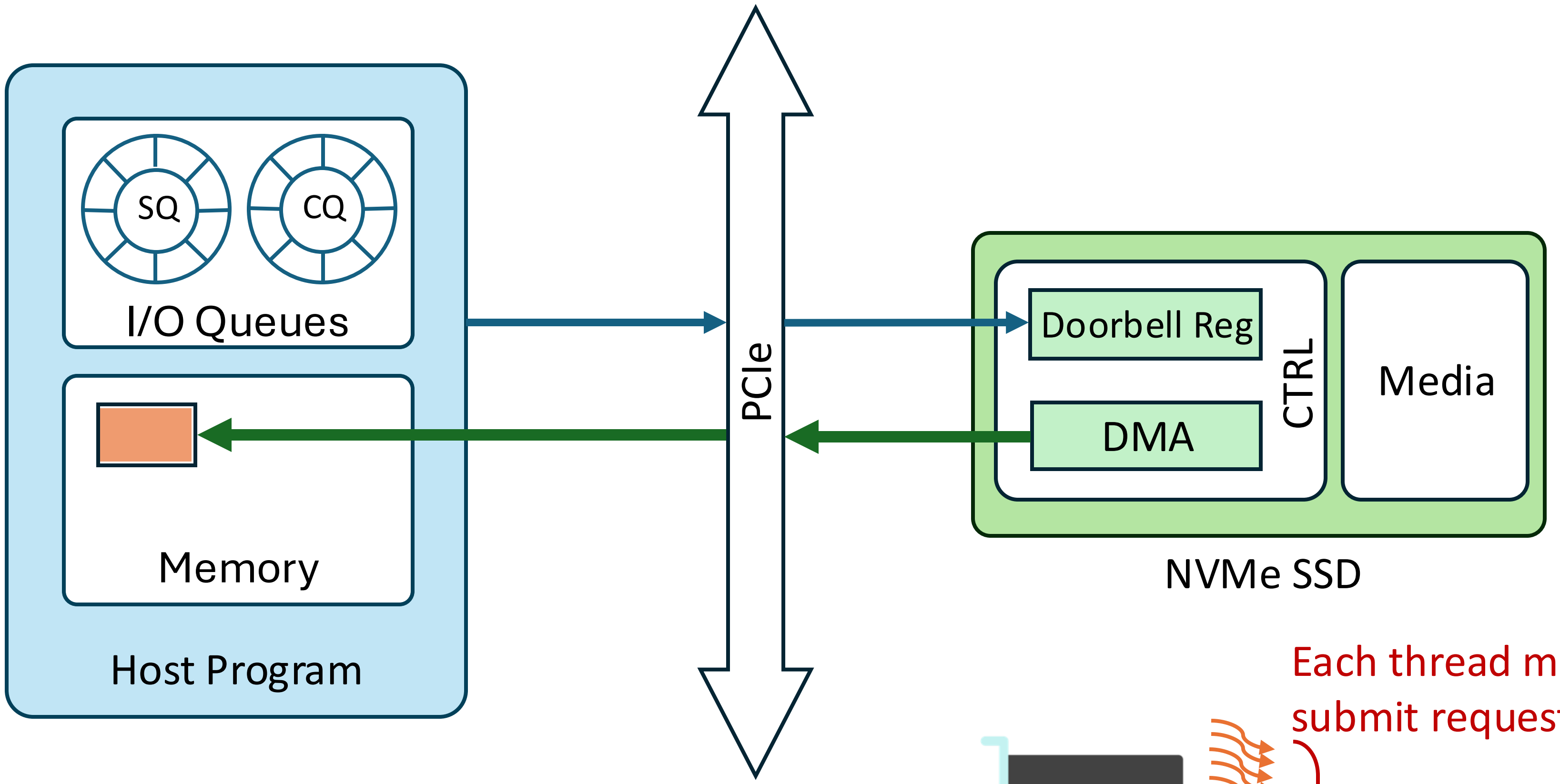


Massive parallel threads

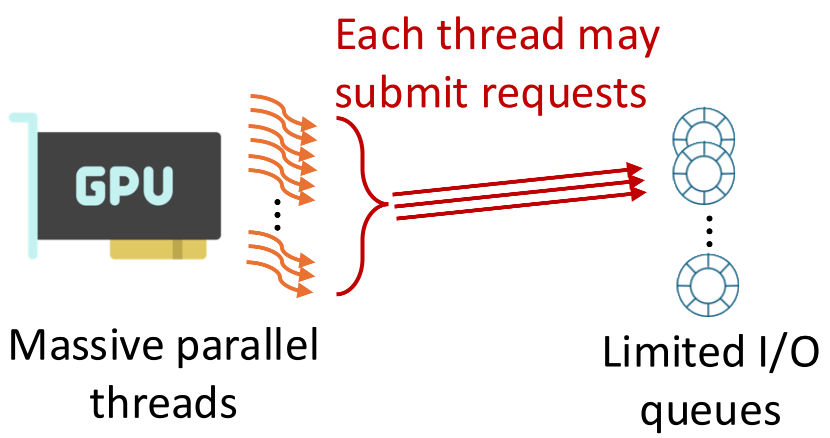


Limited I/O queues

Background of NVMe Protocol



The NVMe protocol is fundamentally asynchronous



Deadlock Risks in Async GPU-Centric NVMe I/O

Async GPU-centric NVMe I/O can easily lead to a deadlock.

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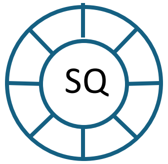

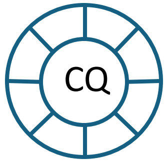

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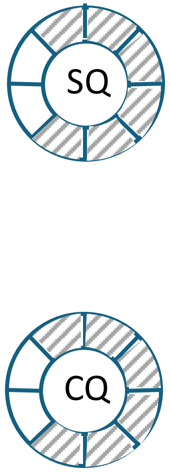

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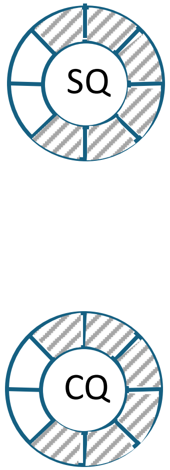
    ...
```



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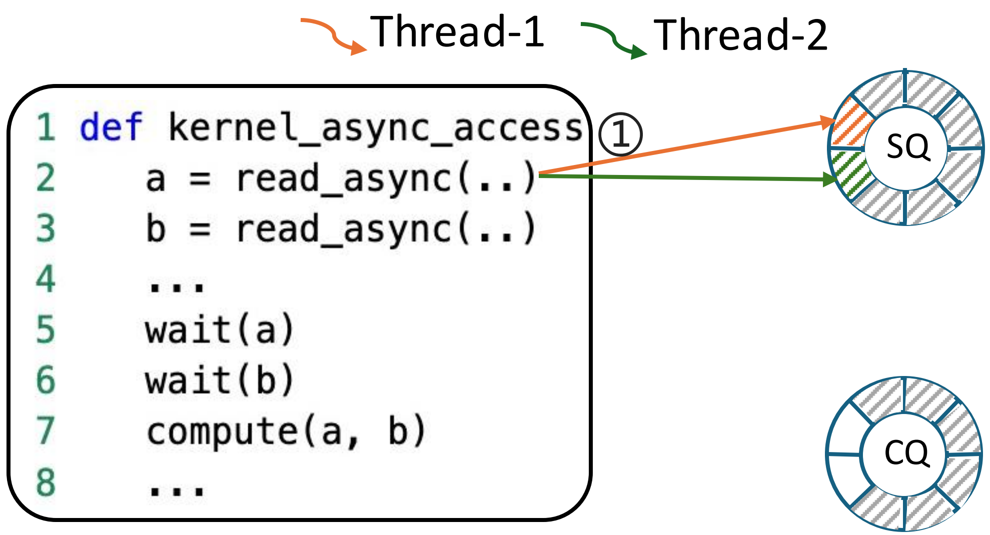

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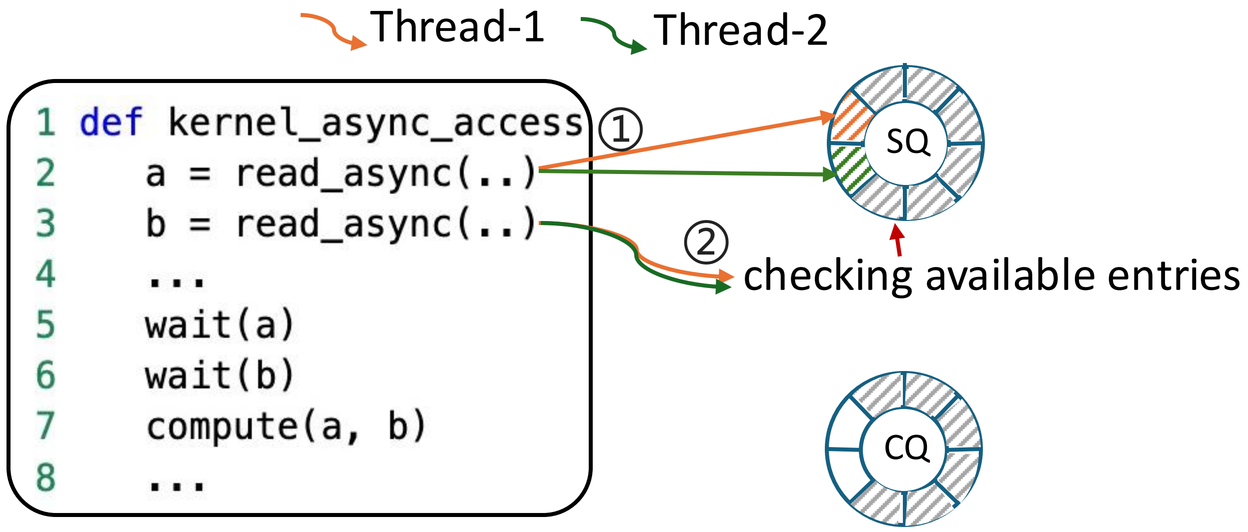

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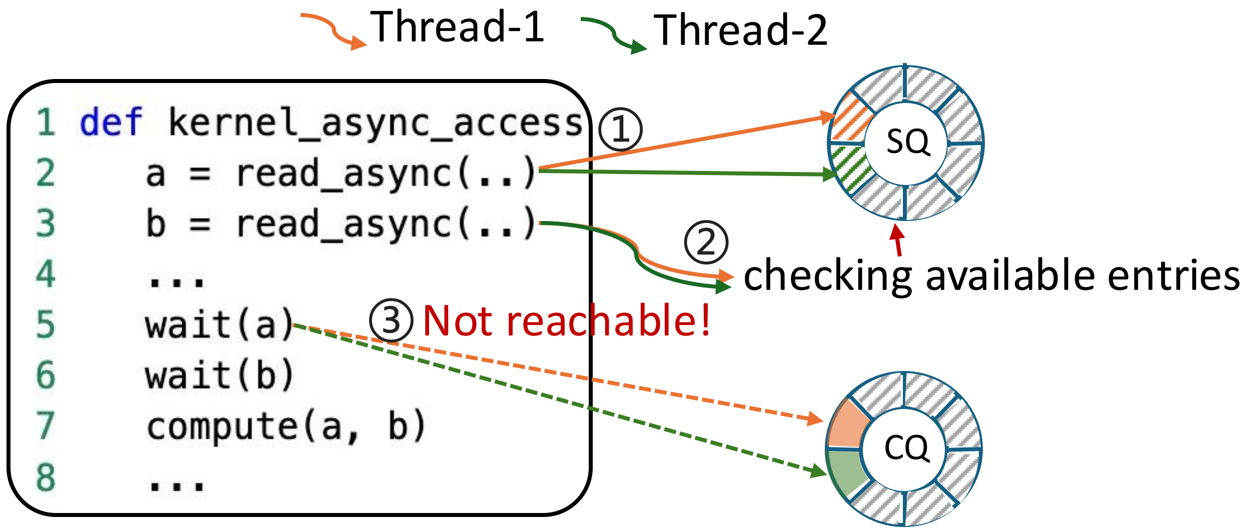

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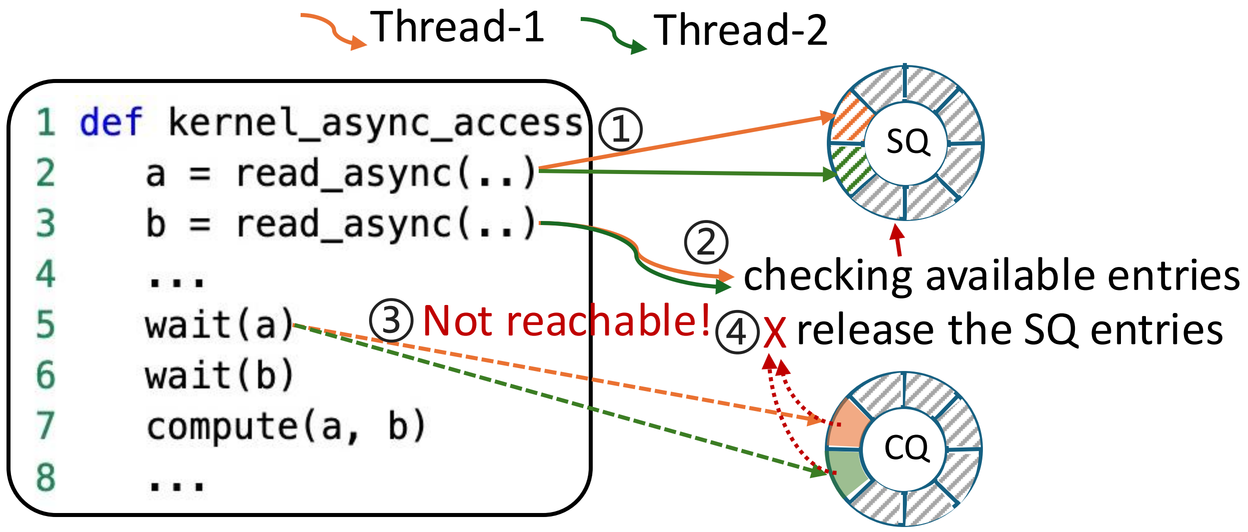

Deadlock Risks in Async GPU-Centric NVMe I/O

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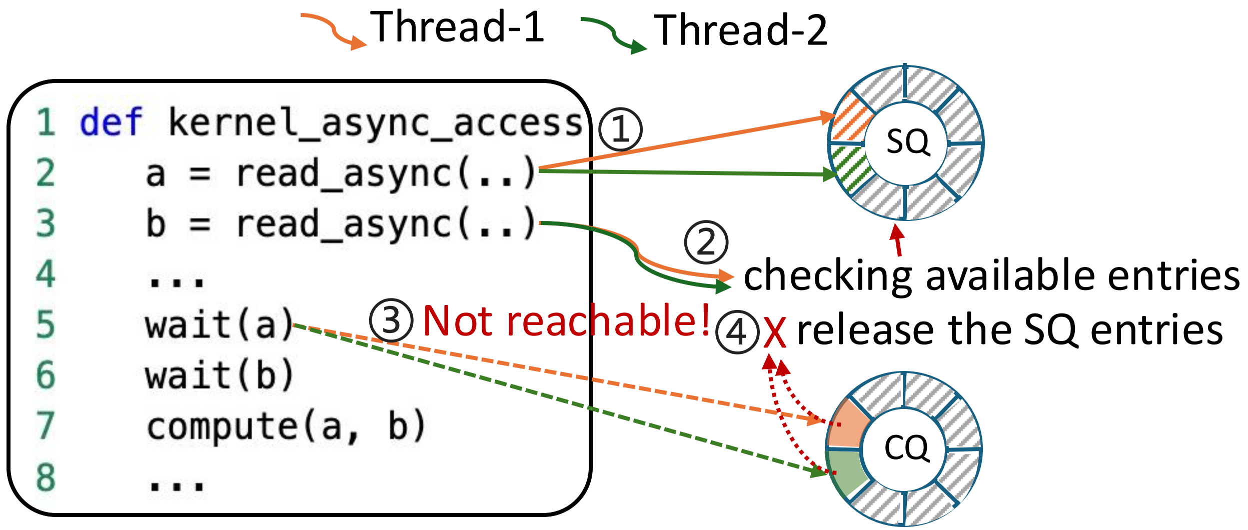

- The root cause of this deadlock is allowing user threads to **hold multiple locks** that can block other user threads. (I/O queues, software cache lines)

AGILE Polling Service

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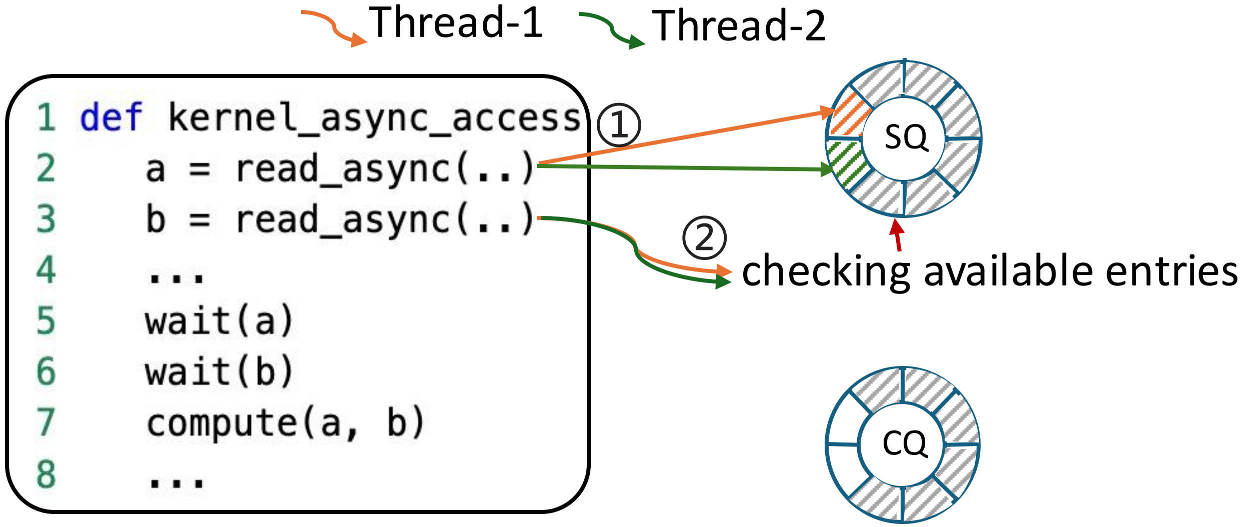
To avoid deadlock from asynchronous NVMe I/O:



AGILE Polling Service

To avoid deadlock from asynchronous NVMe I/O:

- A warp-centric AGILE polling service running in the background

Thread-1 Thread-2

```
def kernel_async_access
    a = read_async(..)
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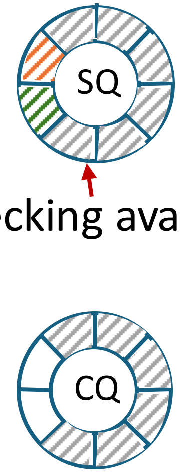
    ...
    wait(a)
    wait(b)
    compute(a, b)
    ...
```



checking available entries

AGILE Polling Service

```
def agile_service
    while(!stop_sig):
        if(poll(...)):
            release_SQE(...)
```

AGILE Polling Service

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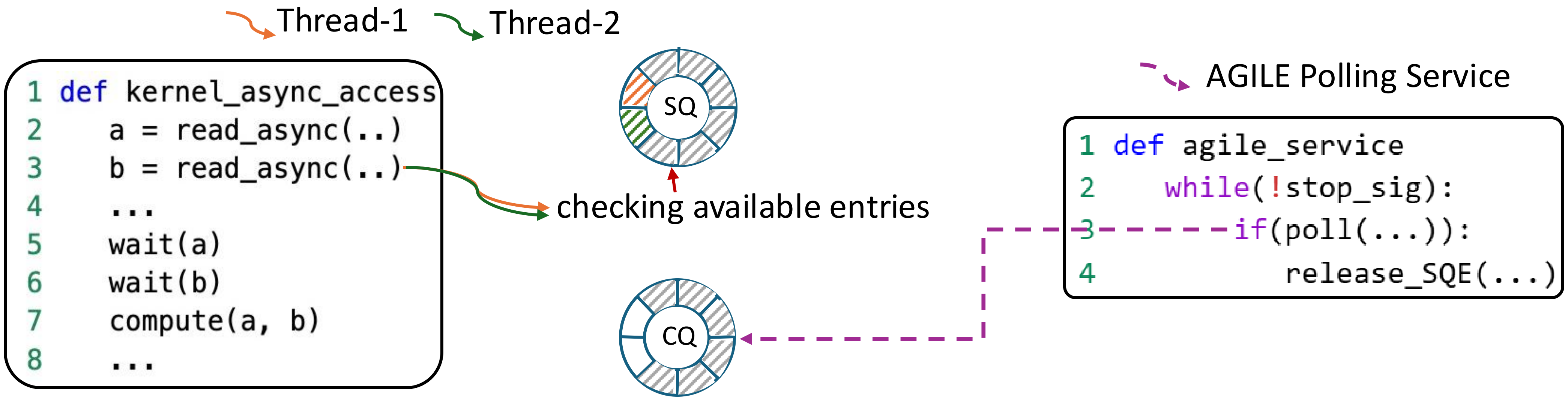

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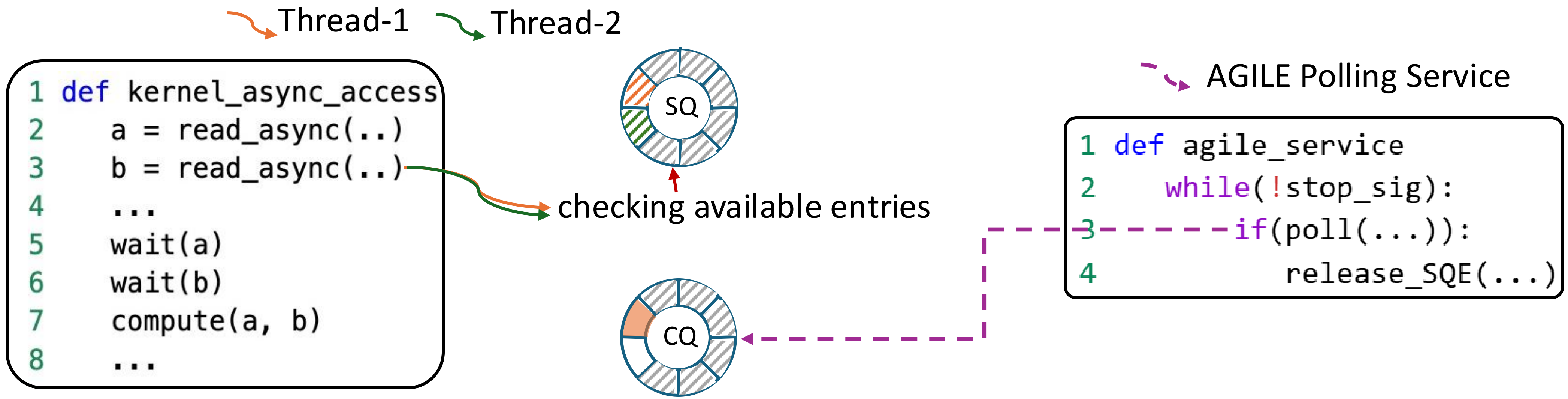

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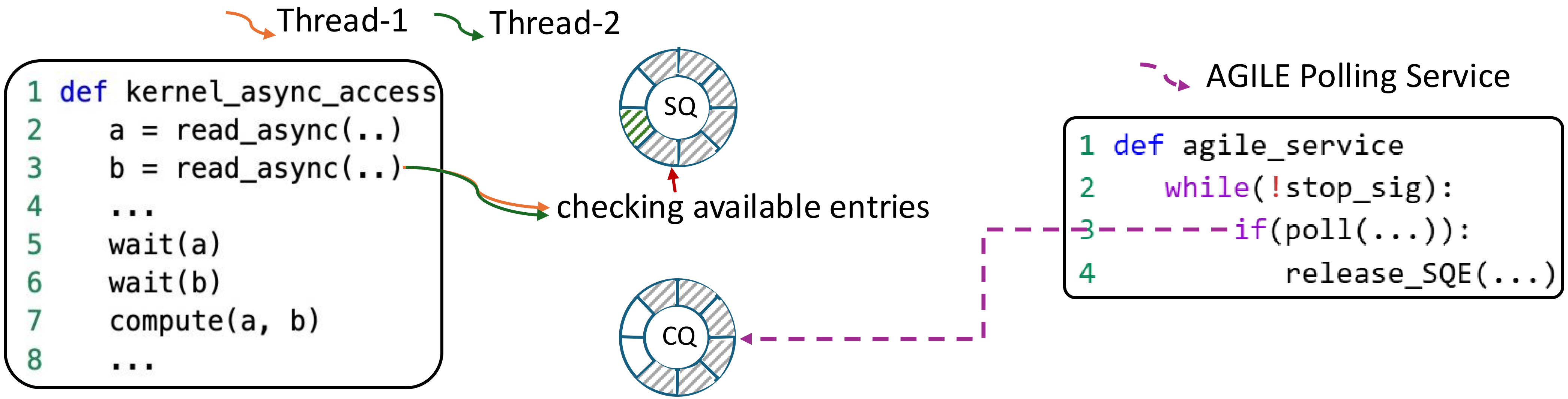

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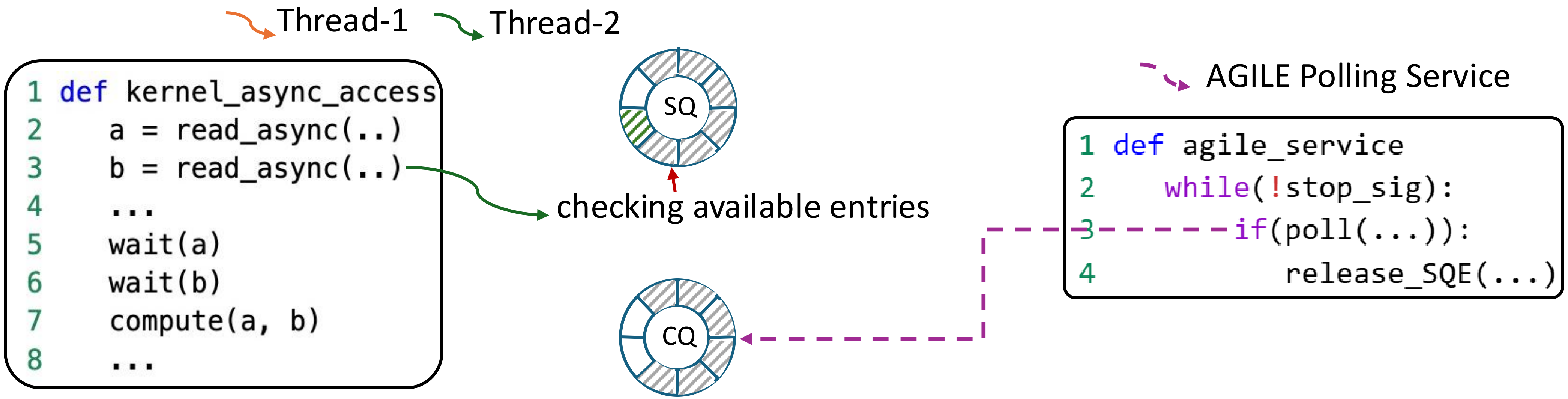

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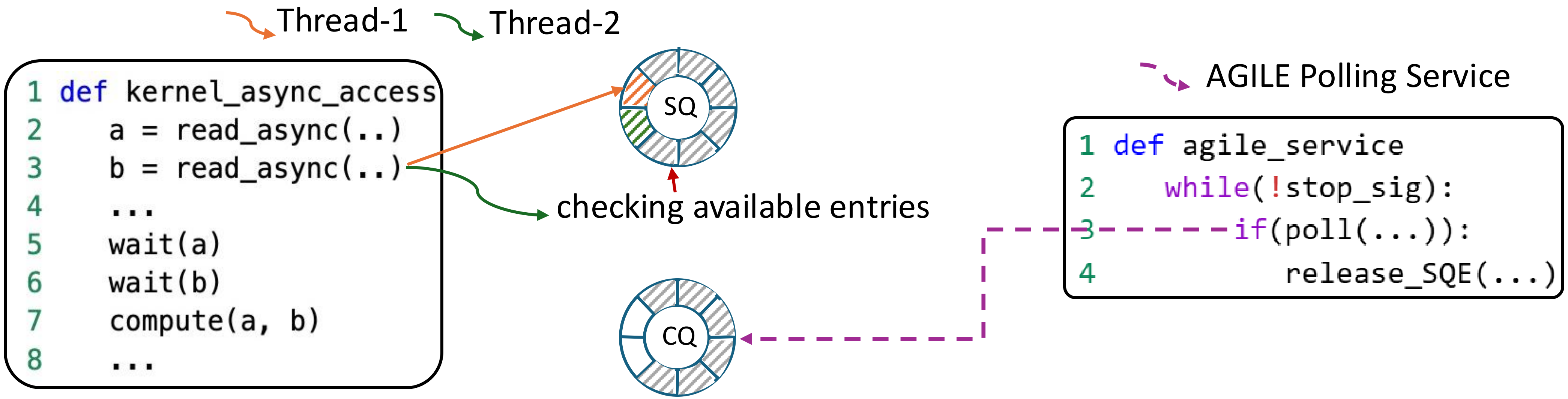

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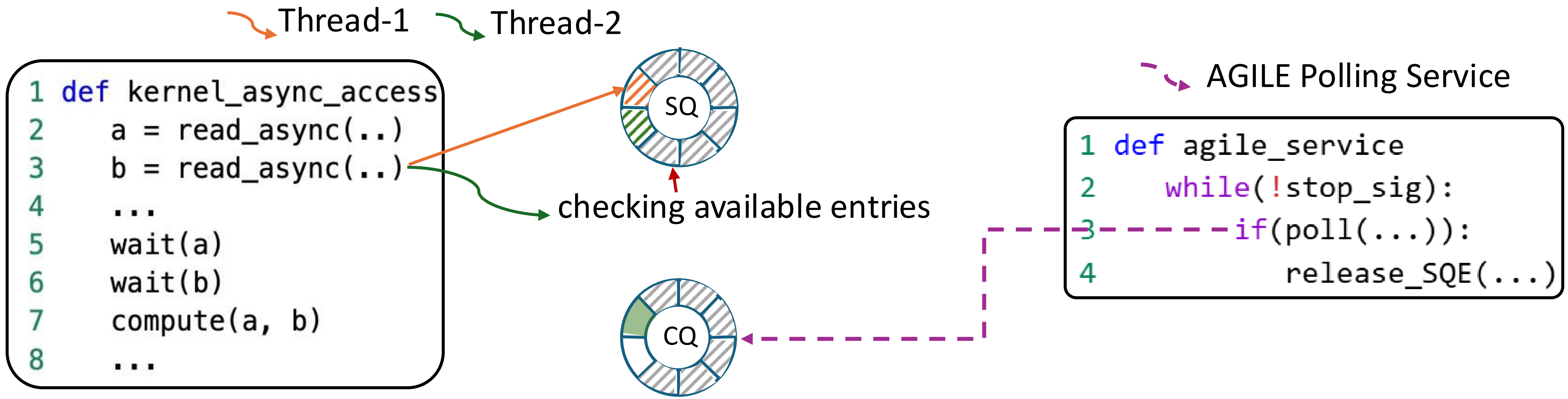

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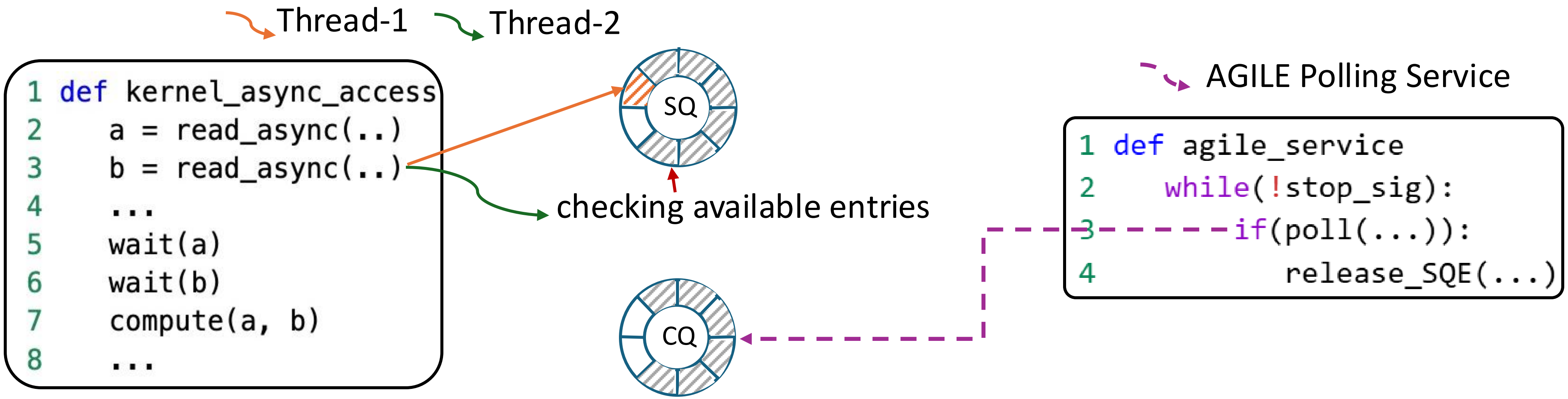

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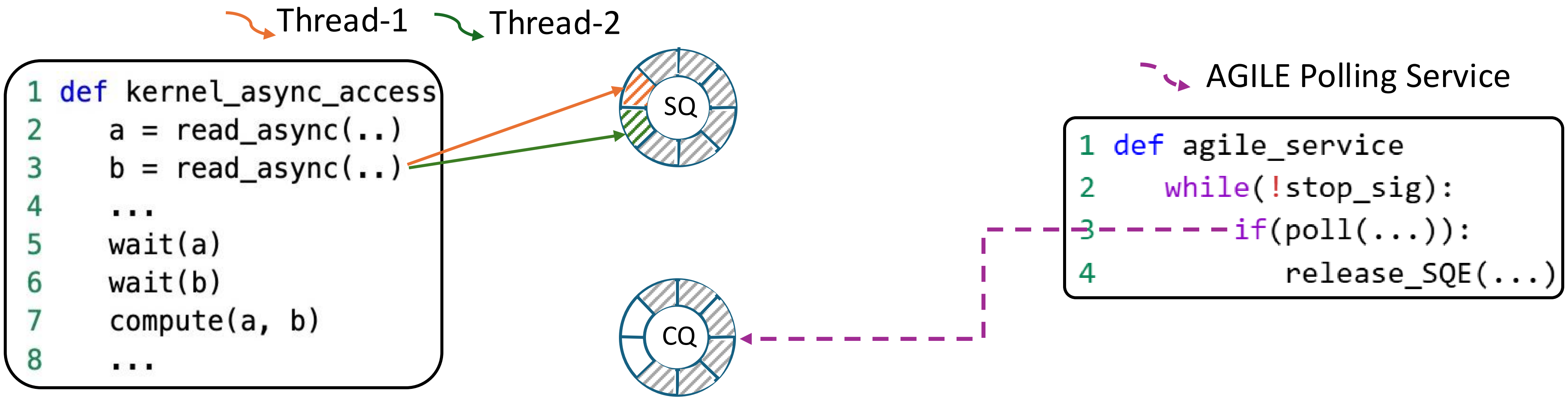

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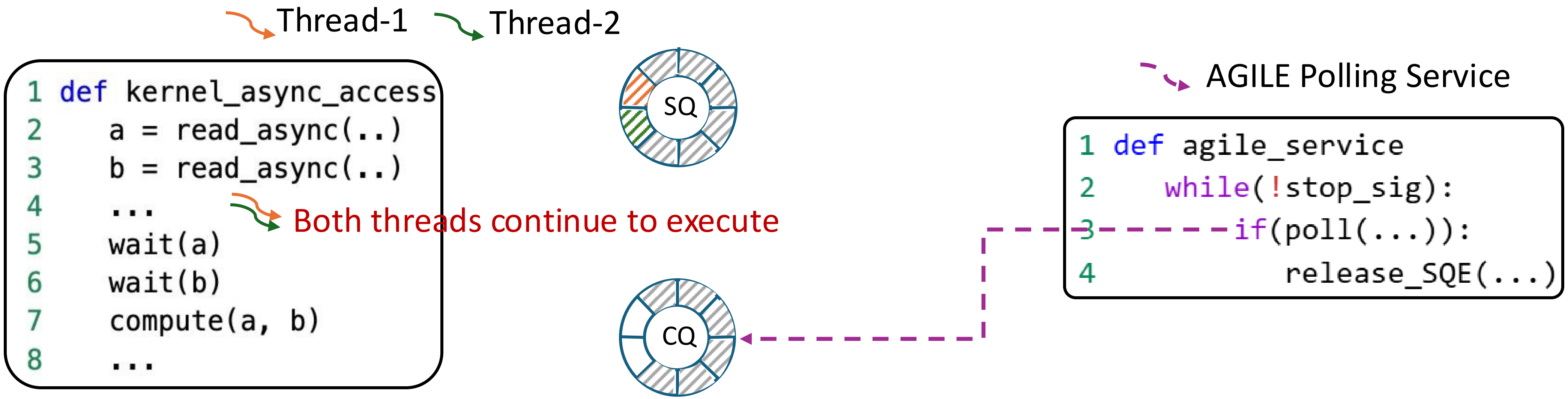

AGILE Software Cache

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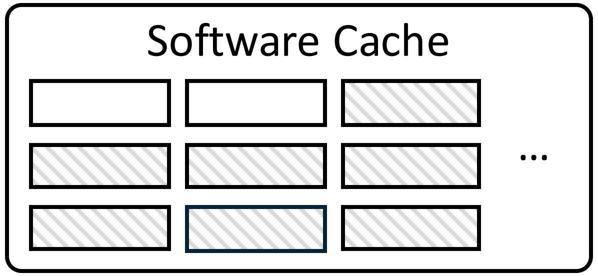

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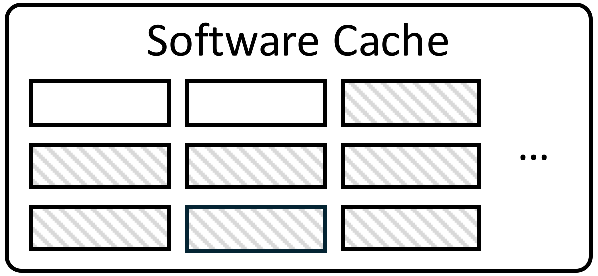

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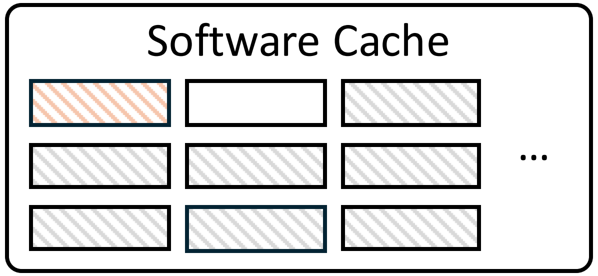

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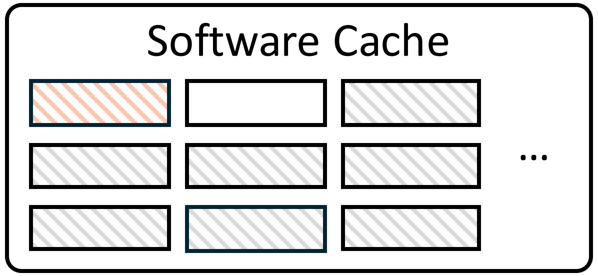

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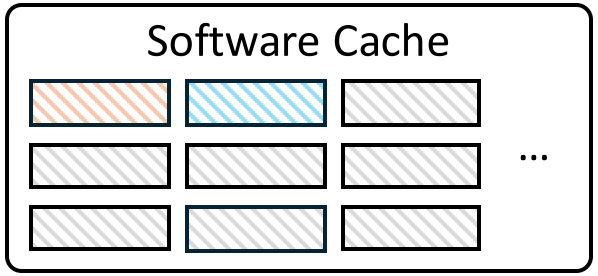

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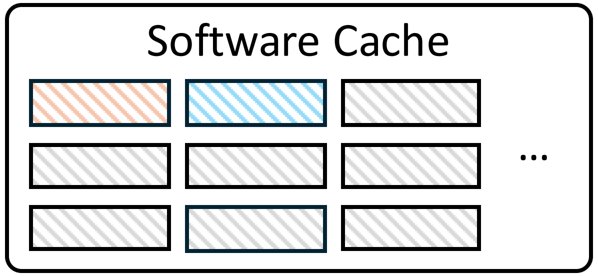

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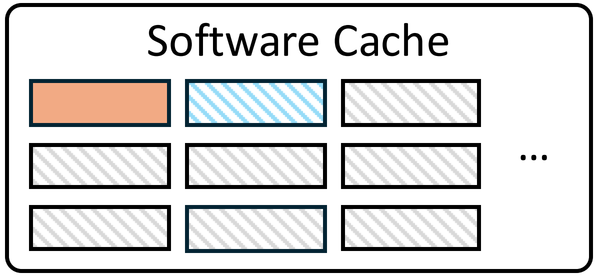

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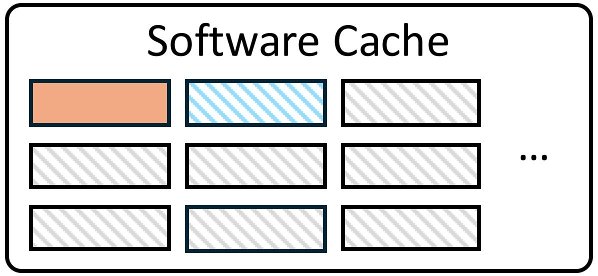

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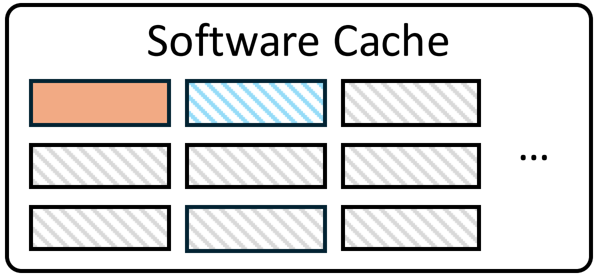

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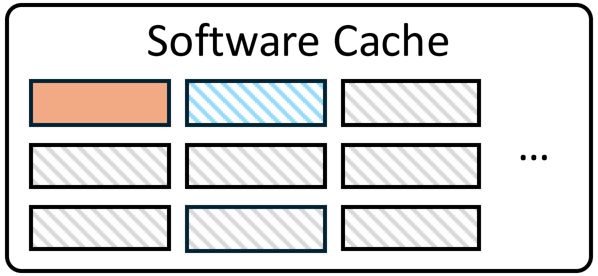

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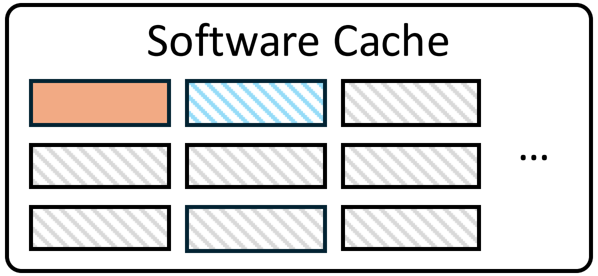
Other threads request new software cache lines



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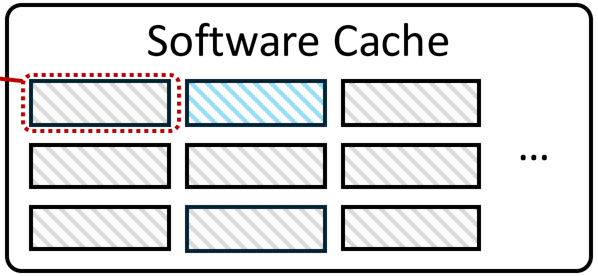
```
1 def kernel_async_access
2     a = read_async(..)
3     b = read_async(..)
4     ...
5     wait(a)
6 →   wait(b)
7     compute(a, b)
8     ...
```

Other threads request new software cache lines

a is evicted at line 6 to avoid blocking others



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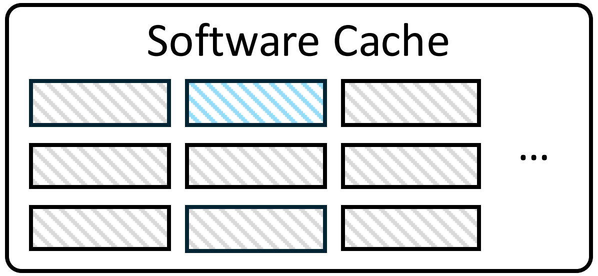

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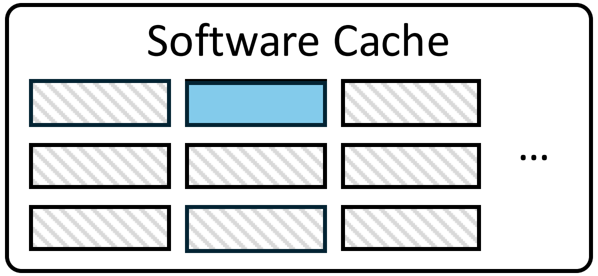

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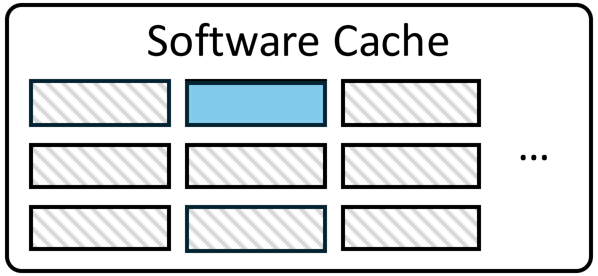

AGILE Software Cache

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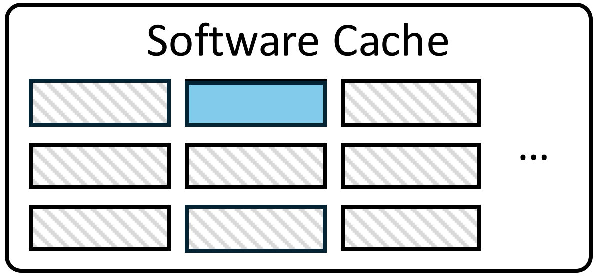
    ...
    wait(a)
    wait(b)
    compute(a, b)
    ...
```

Unavailable again



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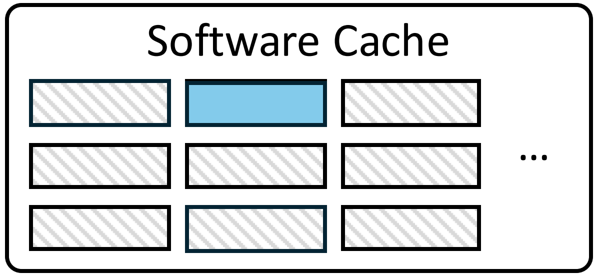
    compute(a, b)
    ...
```

Unavailable again

➢ Use an extra synchronous read when accessing ‘a’



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```

Unavailable again

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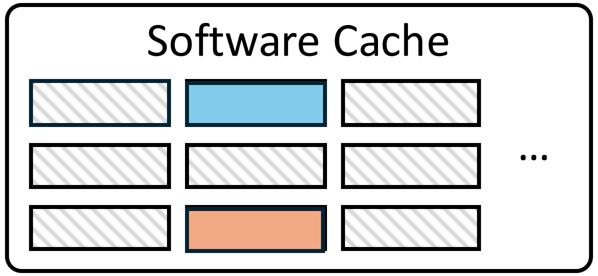

AGILE Software Cache

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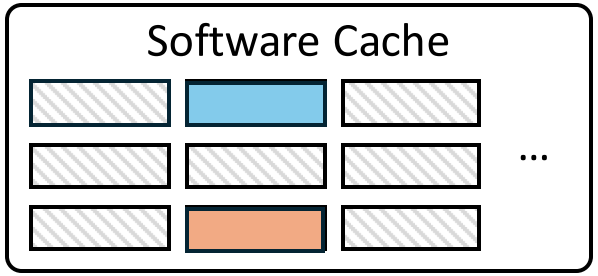
➢ Avoid Deadlocks at the cost of additional I/Os.

```
def kernel_async_access
    a = read_async(..)
    b = read_async(..)
    ...
    wait(a)
    wait(b)
→   compute(a, b)
    ...
```

Unavailable again

➢ Use an extra synchronous read when accessing 'a'



Integrate User-managed Buffers into AGILE

By default, all accesses are proxied by AGILE software cache.

- Requested data may be unavailable again to eliminate deadlocks.

```
def kernel_async_access
    a = read_async(..)
    b = read_async(..)
    ...
    wait(a)
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```

Access via AGILE software cache
(maybe require additional reads)

Integrate User-managed Buffers into AGILE

By default, all accesses are proxied by AGILE software cache.

- Requested data may be unavailable again to eliminate deadlocks.

➢To address this problem, AGILE allows user-managed buffers.

```
def kernel_async_access
    a = read_async(..)
    b = read_async(..)
    ...
    wait(a)
    wait(b)
    compute(a, b)
    ...
```

Access via AGILE software cache
(maybe require additional reads)

```
def kernel_async_access( \
  a_user_buf, b_user_buf):
    read_async(a_user_buf)
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    ...
    a_user_buf.wait()
    b_user_buf.wait()
    compute(a_user_buf, b_user_buf)
    ...
```

Integrate User-managed Buffers into AGILE

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By default, all accesses are proxied by AGILE software cache.

- Requested data may be unavailable again to eliminate deadlocks.

➢ To address this problem, AGILE allows user-managed buffers.

```
def kernel_async_access
    a = read_async(..)
    b = read_async(..)
    ...
    wait(a)
    wait(b)
    compute(a, b)
    ...
```

Access via AGILE software cache
(maybe require additional reads)

User-managed buffers

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Data will not be
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Data will not be evicted once ready.

Data is guaranteed to be ready.

Integrate User-managed Buffers into AGILE

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When multiple threads request the same data, data conflicts may occur.

Integrate User-managed Buffers into AGILE

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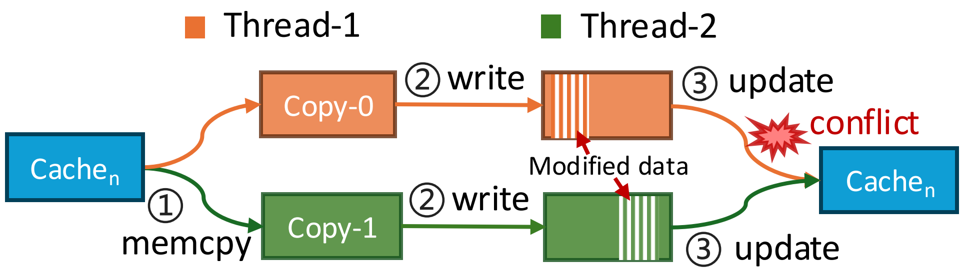

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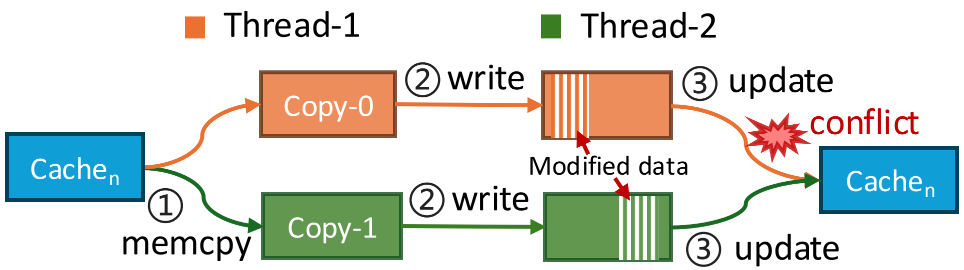

AGILE provides a compile-time optional mechanism (share-table) to let user threads access the same user-managed buffer.

Integrate User-managed Buffers into AGILE

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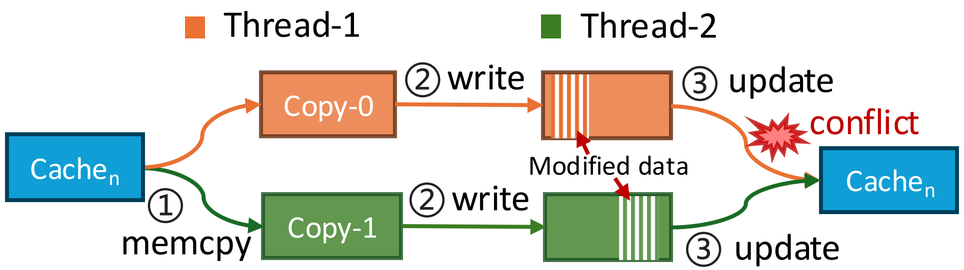

AGILE provides a compile-time optional mechanism (share-table) to let user threads access the same user-managed buffer.

When the share-table is enabled at compile time:

- user-managed buffer (L1; managed by user; registered to share-table)
- Software cache (L2; managed by AGILE)
- SSDs (L3; managed by AGILE)

AGILE's API

```
class GPUCache:public GPUCacheBase<GPUCache>{...};
#define AGILE_CTRL AgileCtrl<GPUCache, ShareTable>
__global__
void kernel(AGILE_CTRL * ctrl, void * data){
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  AgileLockChain chain;

  // Method-1: AGILE prefetch
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Debug option for detecting deadlock

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Init AGILE & Start AGILE service

AGILE's API

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Init AGILE & Start AGILE service

Start user kernel

AGILE's API

Customizing software cache policy

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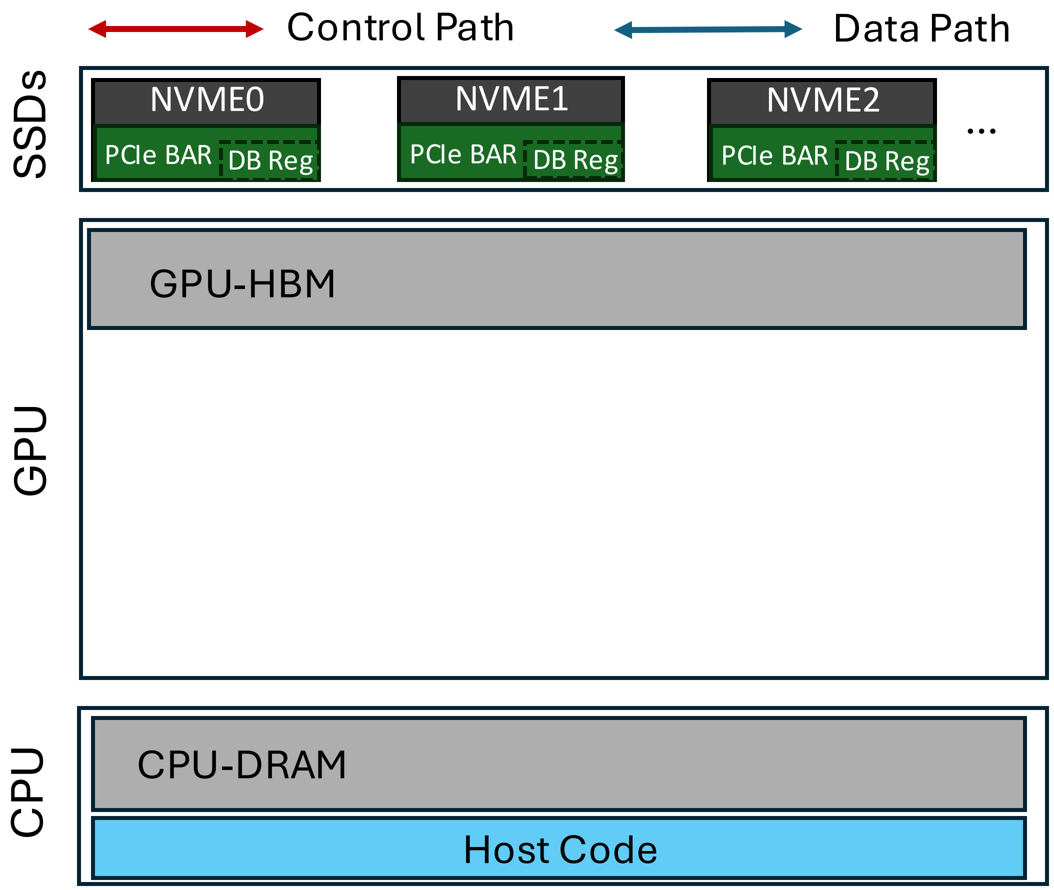
Init AGILE & Start AGILE service

Start user kernel

Stop AGILE service & close SSDs

Summary of AGILE

Feature Highlights:



System overview of AGILE

Summary of AGILE

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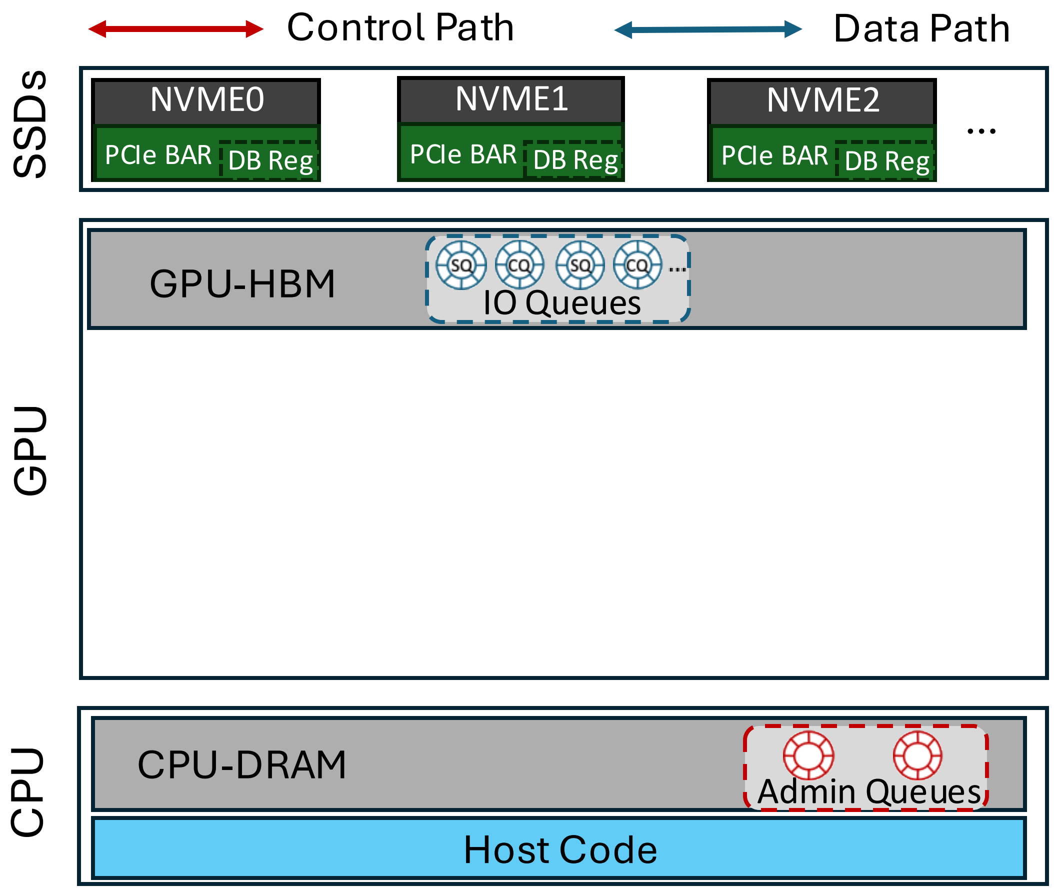

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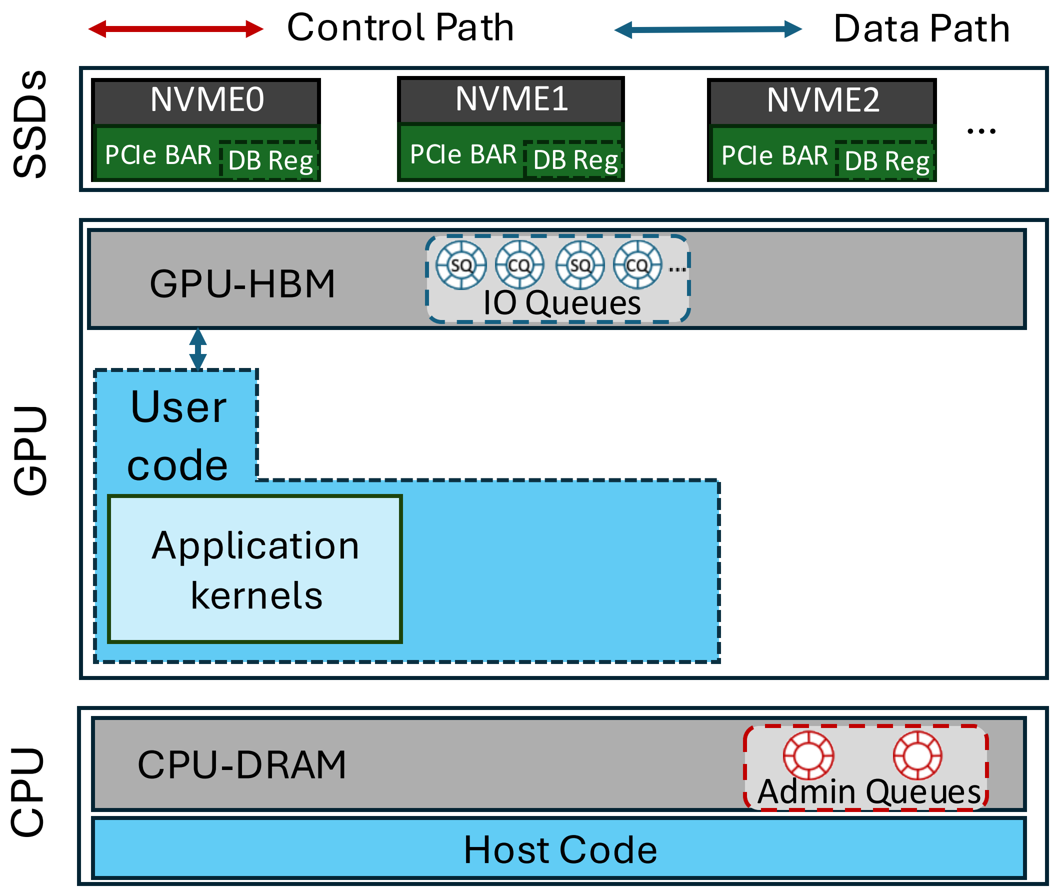
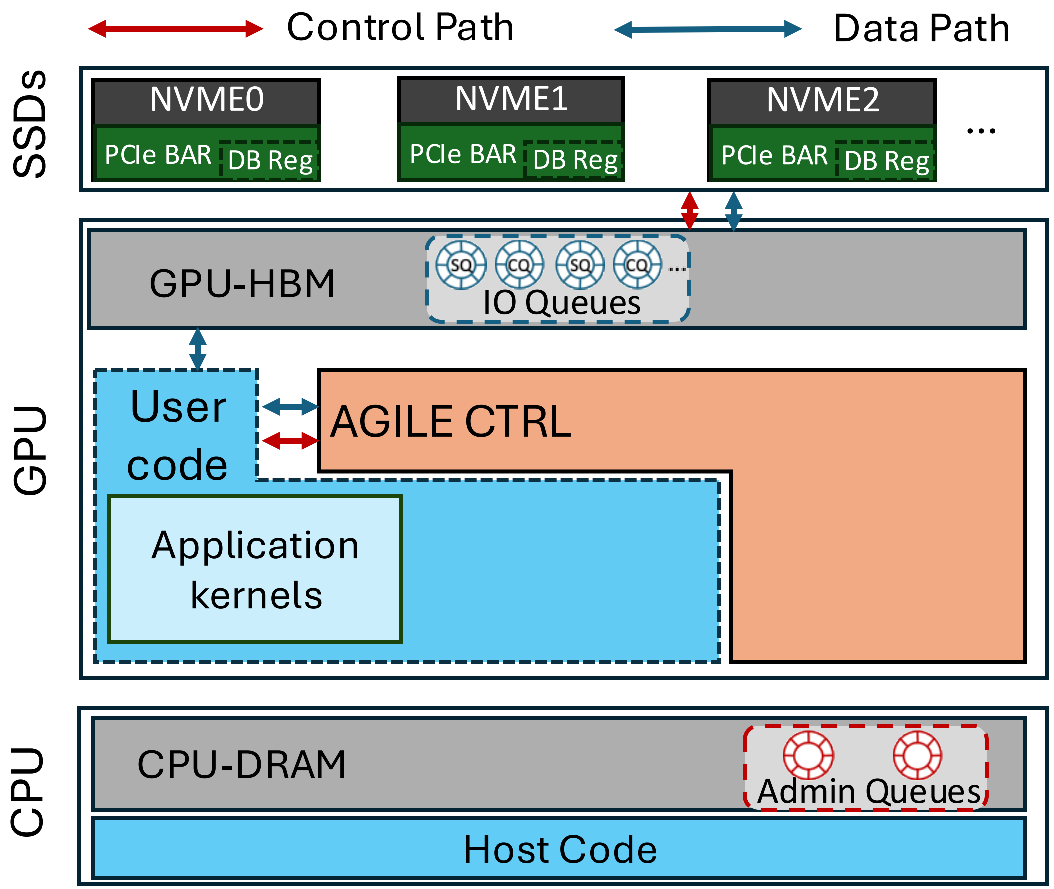


System overview of AGILE

Summary of AGILE

Feature Highlights:

1. AGILE is the first async GPU-centric I/O model, allowing GPU threads to access SSDs asynchronously.



System overview of AGILE

Summary of AGILE

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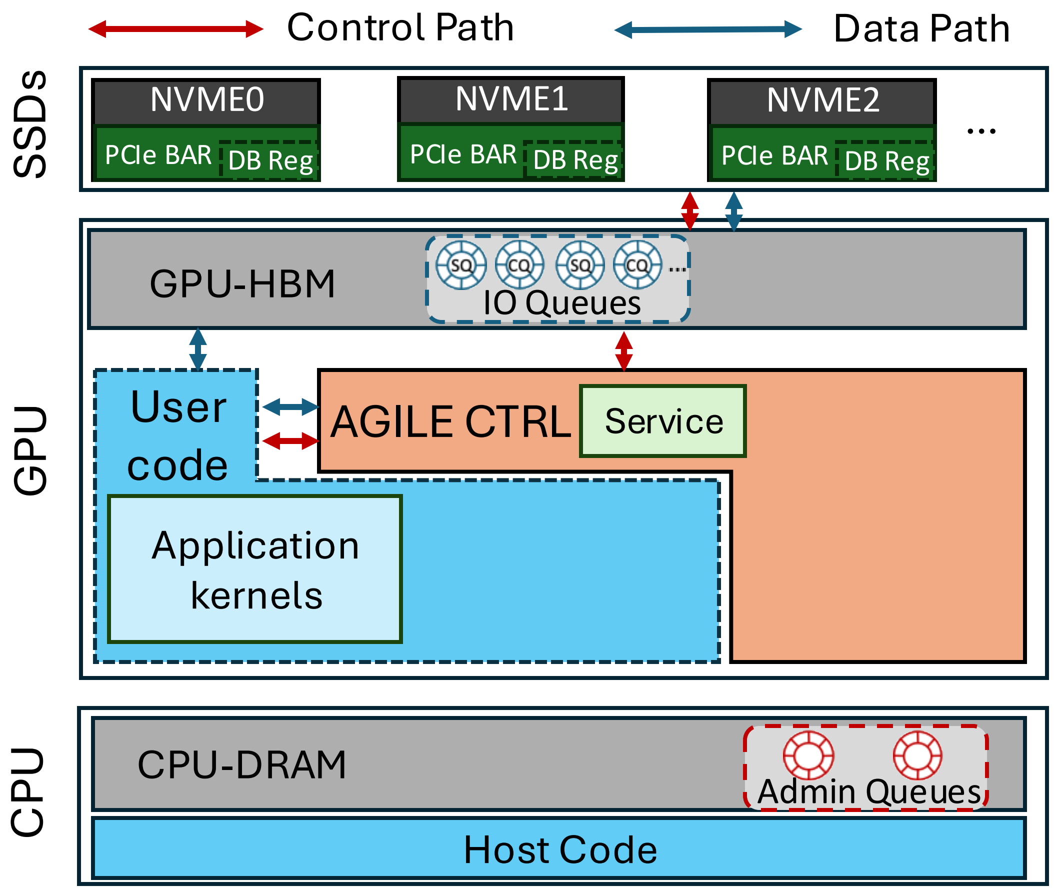

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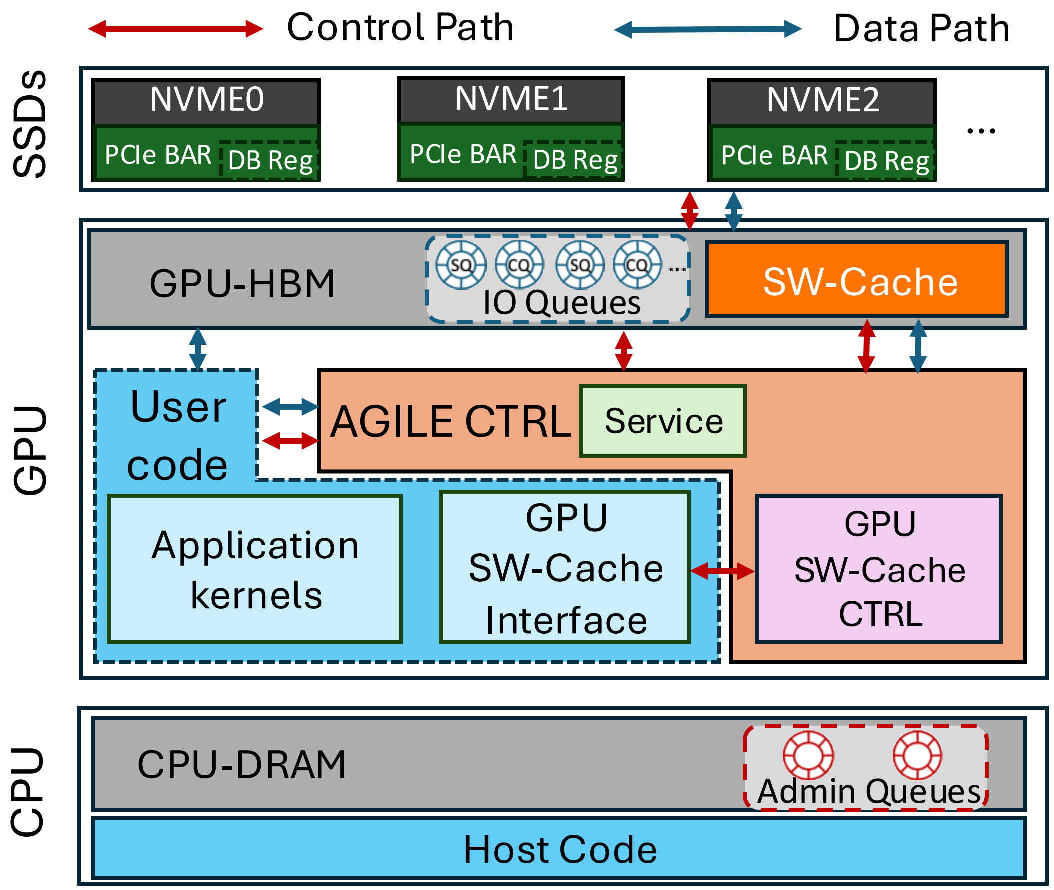

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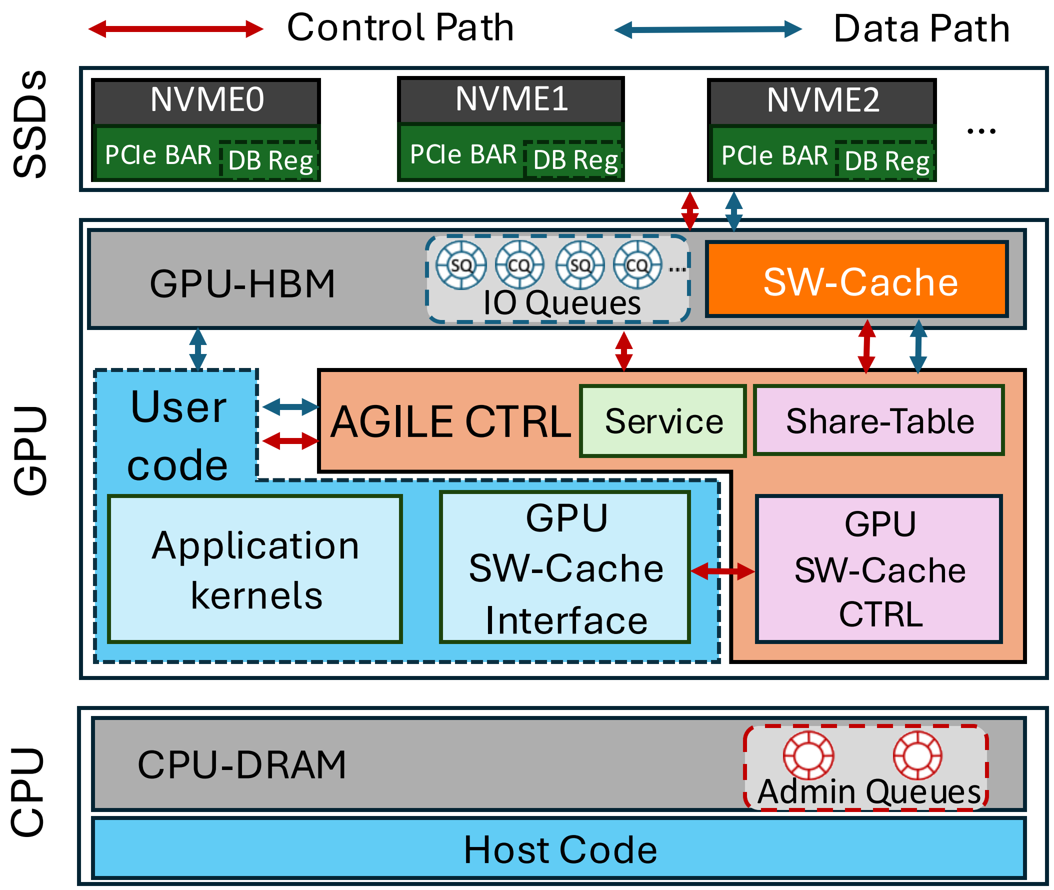
4. AGILE allows user-maintained buffers to be integrated into the software cache hierarchy.



System overview of AGILE

Experimental Setup

- Dell R750 Server
  - Ubuntu 20.04 (Linux 5.4.0-200-generic)
- Nvidia RTX 5000 Ada GPU (PCIe Gen4 x16)
- NVMe SSDs
  - Dell Ent NVMe AGN MU AIC 1.6TB SSD (PCIe Gen4 x4)
  - Two Samsung 990 PRO 1TB SSDs (PCIe Gen4 x4)
- Software Cache Policy
  - Clock replacement algorithm[1] (keep the same with BaM)

[1] F. J. Corbato. 1968. A Paging Experiment With The Multics System. Technical Report, Massachusetts Institute of Technology, Cambridge, Project MAC (1968).

Experimental Evaluation

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1. Compute and communication overlap.

- 1 thread block issues 64 NVMe commands, and uses fetched data for compute.

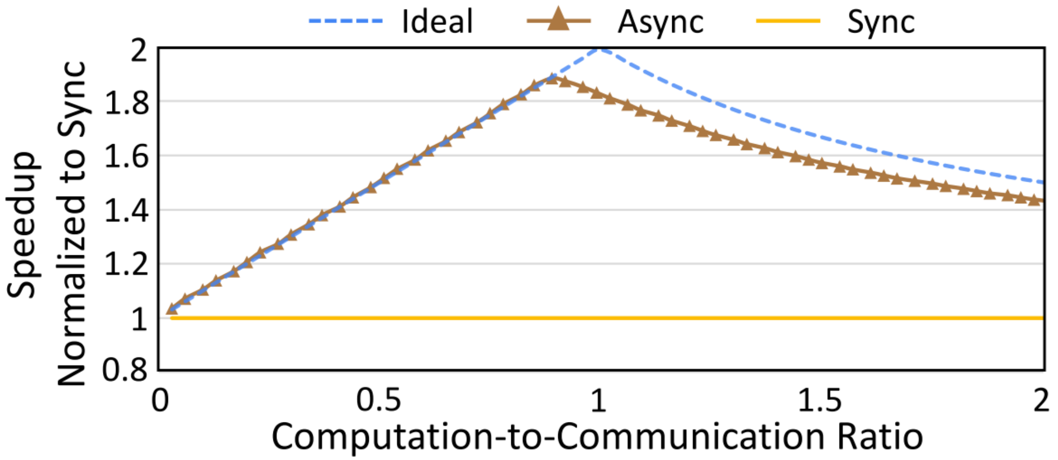

Figure 4: Speedup comparison of asynchronous I/O over synchronous I/O on workloads with different Computation-to-Communication Ratio (CTC).

Experimental Evaluation

1. Compute and communication overlap.
   - 1 thread block issues 64 NVMe commands, and uses fetched data for compute.

➢AGILE can hide slow communication with computation effectively.

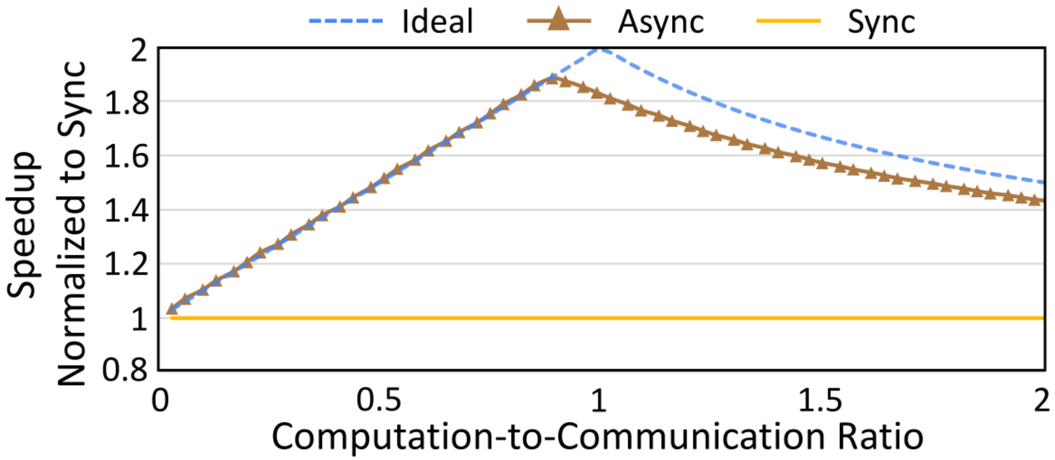

Figure 4: Speedup comparison of asynchronous I/O over synchronous I/O on workloads with different Computation-to-Communication Ratio (CTC).

Experimental Evaluation

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2. Scalability in 4KB random read/write
   - Access different SSDs in an interleaving fashion.

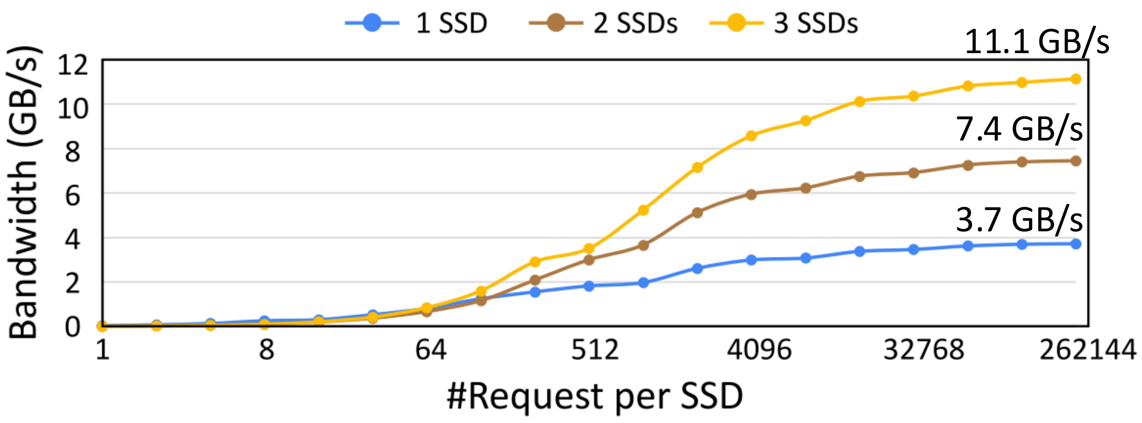


Figure 5: AGILE 4KB random read on multiple SSDs

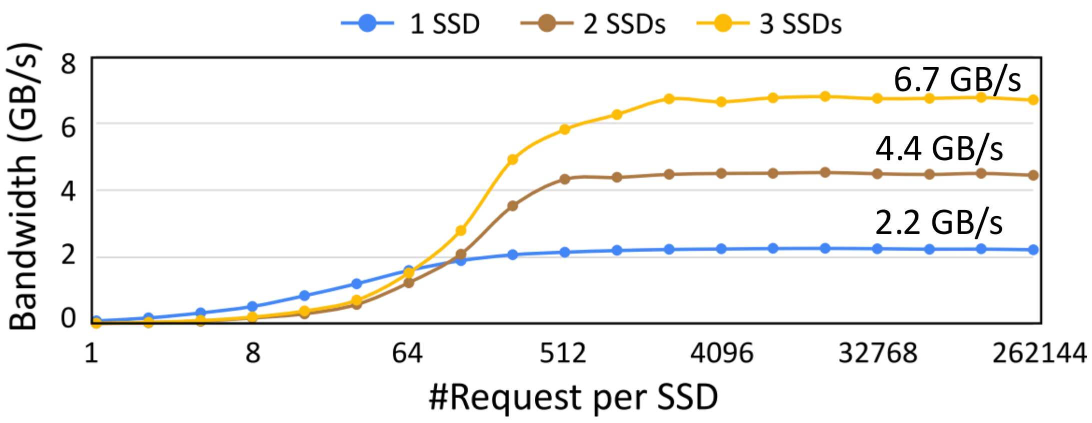
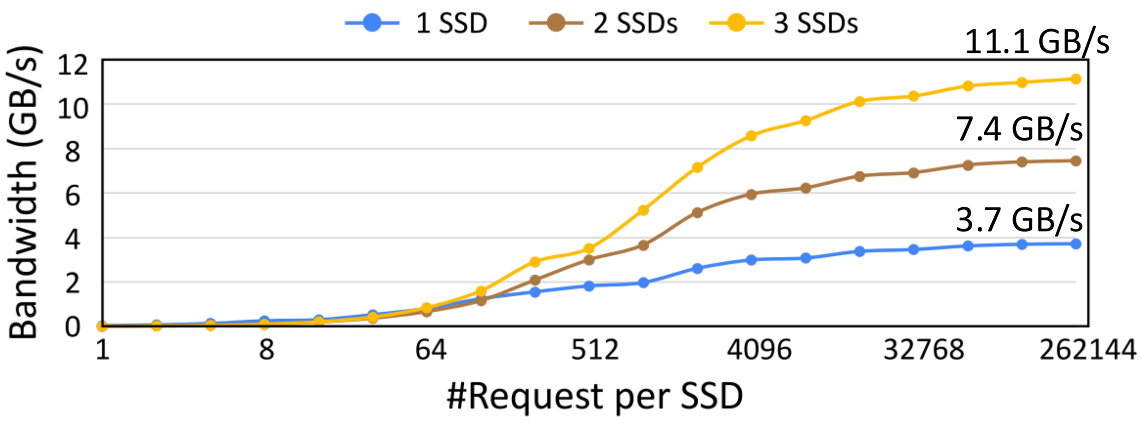


Figure 6: AGILE 4KB random write on multiple SSDs

Experimental Evaluation

2. Scalability in 4KB random read/write
   - Access different SSDs in an interleaving fashion.

➢AGILE shows good scalability.



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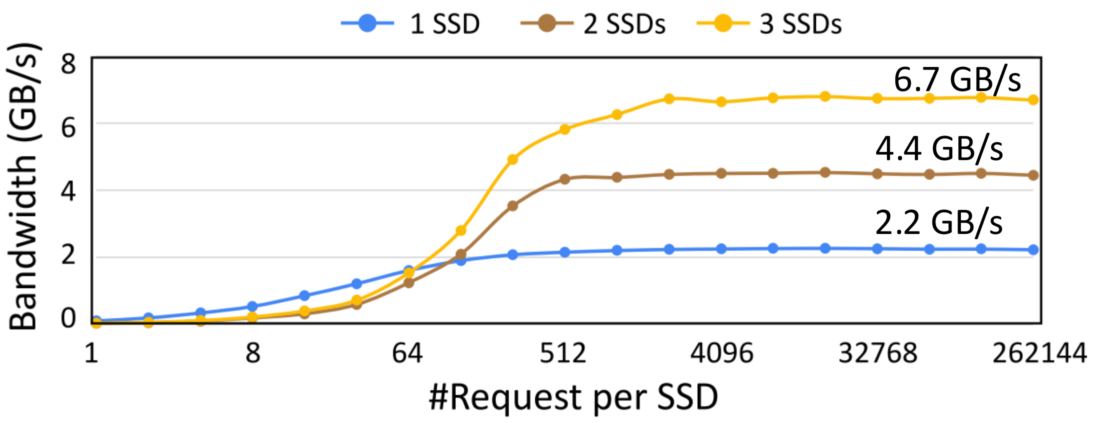

Figure 6: AGILE 4KB random write on multiple SSDs

Experimental Evaluation

3. Comparison with BaM on DLRM inference MicroBenchmark.

- The DLRM model is adopted from [1] with Criteo 1TB Click Logs dataset[2].
- cuBLAS is used for all matrix multiplications.
- BaM and AGILE are used for fetching data.
- AGILE is used in both synchronous mode and asynchronous mode

[1] Naumov, Maxim, et al. "Deep learning recommendation model for personalization and recommendation systems." *arXiv preprint arXiv:1906.00091* (2019).
[2] Criteo AI Lab. 2025. Download Criteo 1TB Click Logs dataset - Criteo AI Lab. https://ailab.criteo.com/download-criteo-1tb-click-logs-dataset/

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- Sweep key parameter: Batch Size & the Number of I/O Queues.

Default parameters:
- Batch Size: 2048
- #I/O queues: 128
- Software cache size: 2 GB

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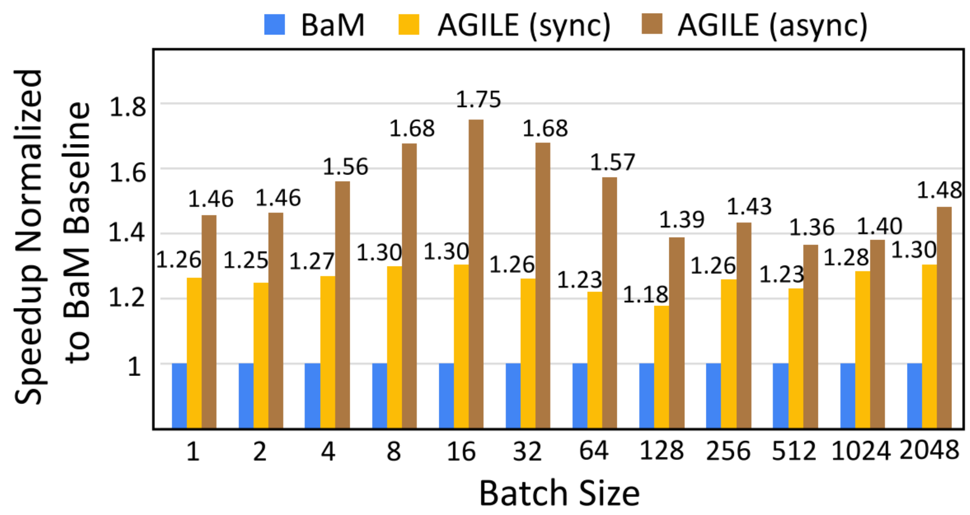

Figure 8: Speedup comparison of AGILE (async and sync modes) and BaM across varying batch sizes in DLRM inference.

[1] Naumov, Maxim, et al. "Deep learning recommendation model for personalization and recommendation systems." *arXiv preprint arXiv:1906.00091* (2019).
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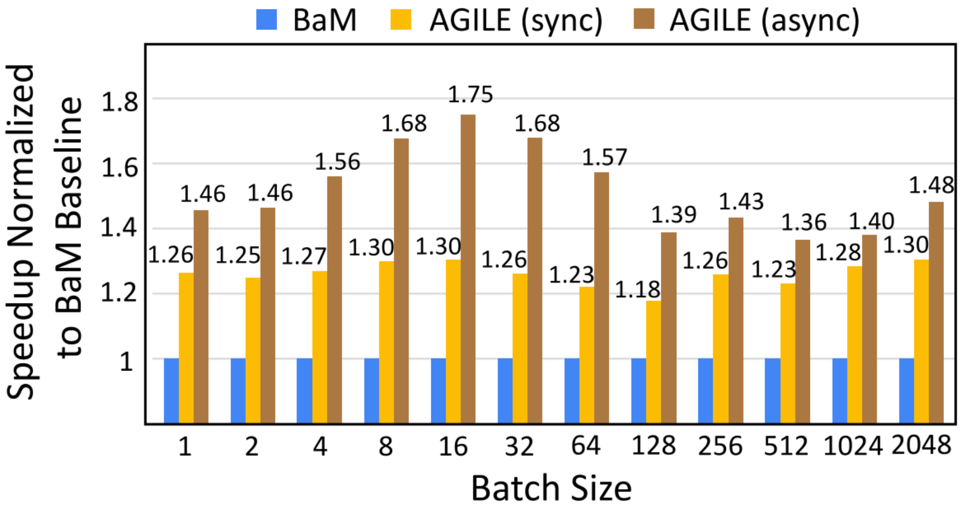

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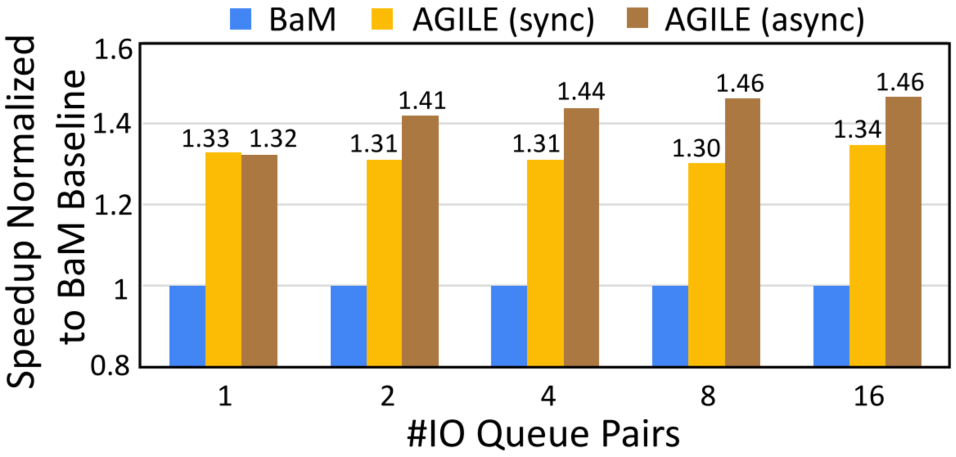

Figure 9: Speedup comparison of AGILE (async and sync modes) and BaM under varying numbers of I/O queue pairs in DLRM inference.

[1] Naumov, Maxim, et al. "Deep learning recommendation model for personalization and recommendation systems." *arXiv preprint arXiv:1906.00091* (2019).
[2] Criteo AI Lab. 2025. Download Criteo 1TB Click Logs dataset - Criteo AI Lab. https://ailab.criteo.com/download-criteo-1tb-click-logs-dataset/

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- Software cache size: 2 GB

▪ Sweep key parameter: Software Cache Size

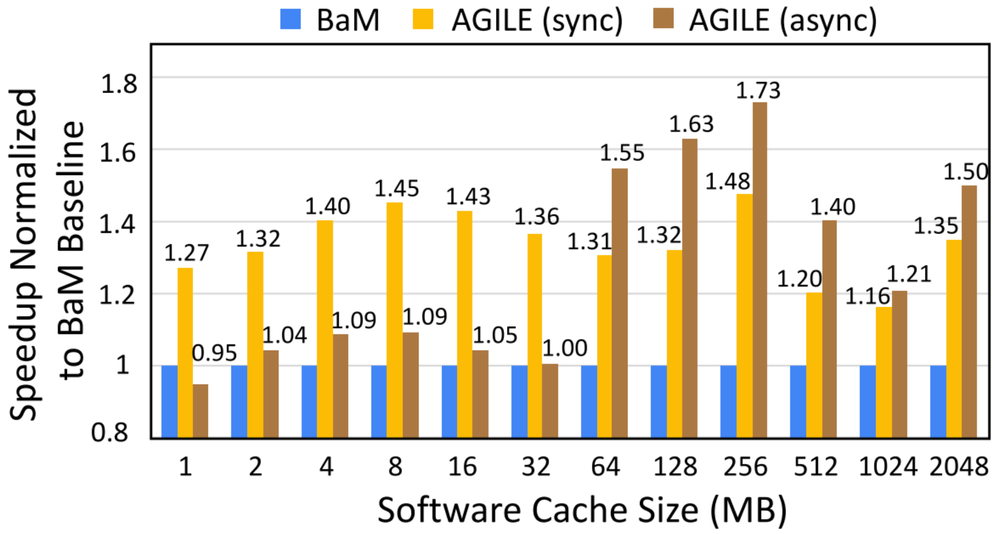

Figure 10: Speedup comparison of AGILE (async and sync modes) and BaM under varying software cache sizes in DLRM inference.

[1] Naumov, Maxim, et al. "Deep learning recommendation model for personalization and recommendation systems." *arXiv preprint arXiv:1906.00091* (2019).

[2] Criteo AI Lab. 2025. Download Criteo 1TB Click Logs dataset - Criteo AI Lab. https://ailab.criteo.com/download-criteo-1tb-click-logs-dataset/

Thank You!

Questions?

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peipei_zhou@brown.edu

AGILE is open source!

https://peipeizhou-eecs.github.io/

https://github.com/arc-research-lab/AGILE

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